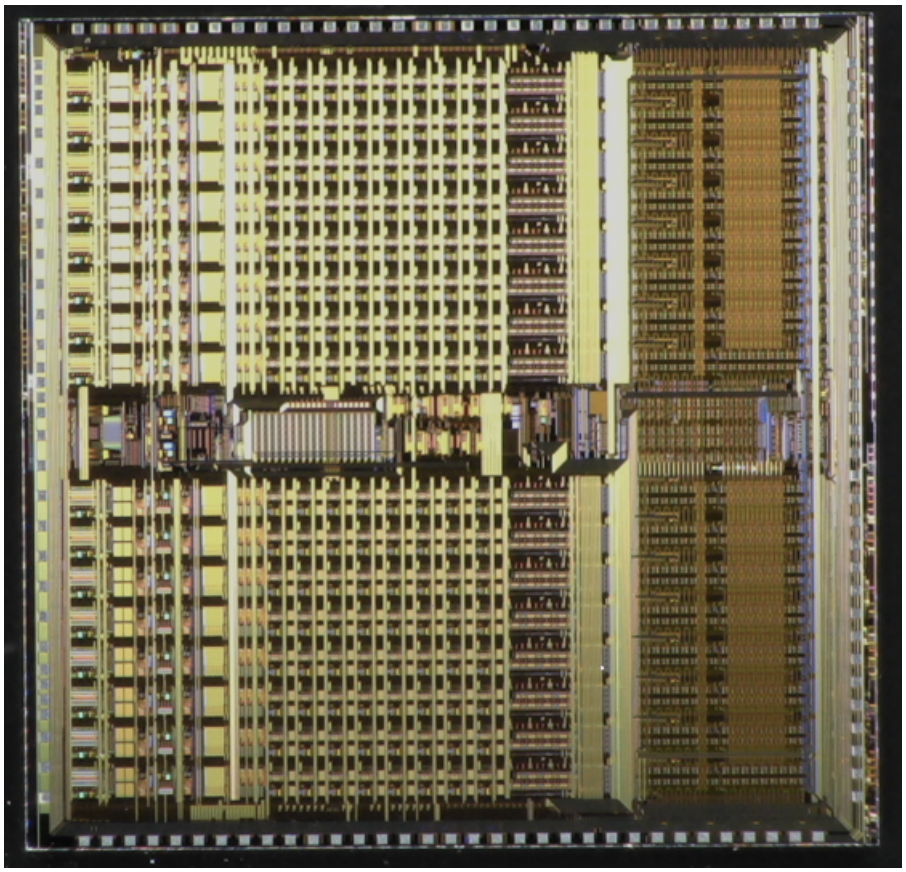
MCI ASIC

Data Sheet

Doc ID	:	D-SA_MCI_DS-3.6
Version	:	1
Revision	:	A
Date	:	June 6, 2019
Classification	:	For Public Release

SPACE-ASICS SA
Didotou 9,
Athens, 10680 Greece
Tel:+30-210-3256993
Fax: +30-210-3256996
Mail: info@space-asics.gr
Web: www.space-asics.gr



REVISION HISTORY

Revision	Date	Comments
Version 1.a	June 6, 2019	Original Version.

Contents

List of Acronyms

ADC	Analog to Digital Converter
AFE	Analog Front END
ASIC	Application Specific Integrated Circuit
BIST	Built In Self Test
CCD	Charged Coupled Device
CQFP	Ceramic Quad Flat Package
DAC	Digital to Analog Converter
DNL	Differential Non-Linearity
EM	Engineering Model
ENOB	Effective Number Of Bits
ESD	Electrostatic discharge
INL	Integral Non-Linearity
LET	Linear Energy Transfer
LT	Lifetime
OVP	Over-Voltage Protection
POR	Power On Reset
PTAT	Proportional to absolute temperature
SA	SPACE-ASICS
SEE	Single Event Effect
SEL	Single Event Latch-up
SEU	Single Event Upset
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
SRR	System Requirements Review
T	Temperature
TBD	To be determined
TID	Total Ionizing Dose
TMR	Triple Mode Redundant

Introduction

This document presents information on the EM MCI ASIC.

1 Functionality

The MCI ASIC is a multichannel CCD and CMOS sensor read out integrated circuit consisting of 16 parallel channels. Each channel contains:

- One Over-Voltage Protection (OVP) unit.
- A clamp unit.
- A selector for selecting the input to the signal chain.
- A Correlated Double Sampler (CDS) unit.
- An offset compensation DAC.
- A Programmable Gain Amplifier (PGA) unit.
- A 12 bit ADC.
- A test DAC that will assist in testing the ADC.
- A test pattern unit that will output data in test mode to assist in verifying the correct functionality of the serializer unit.

2 Block Diagram

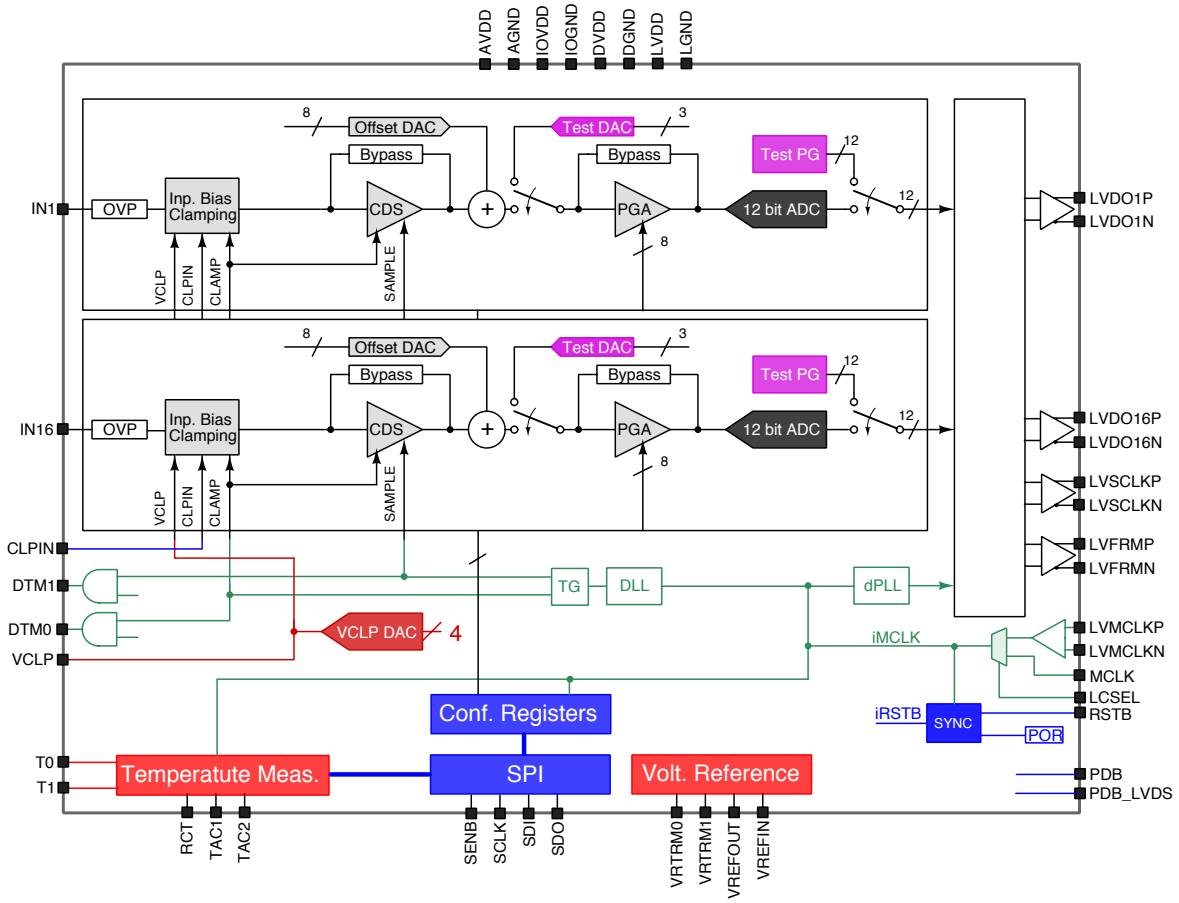


Figure 1: Block diagram of the MCI ASIC.

Features

- Sampling rate from 3 to 20 MSPS
- 16 channel serial LVDS output
- On chip DLL to handle reference and video level sampling signals
- Ability to measure CCD and on chip temperature
- Power down Mode
- Programmable through an SPI interface

Key Characteristics

- 0.25μm TSMC Bulk CMOS Fabrication Technology
- Wide Temperature Operating range (-55 to 125 deg C)
- Radhard up to 300 Krad
- Immune to SELs at 64 MeV/mg/cm^2 (TBC)
- No SEFIs up to 64 MeV/mg/cm^2 (TBC)
- SEU LET threshold above 40 MeV/mg/cm^2 (TBC)
- Test Coverage: 98.5 % min
- Useful life: 15 years min

3 Operation Characteristics

3.1 Analog Channels Sampling

The ASIC has the following configurations:

- The sampling frequency can be configured from 3 to 20 MSPS. The sampling frequency is directly related to the master clock input.
- The CDS functionality can be either activated or de-activated. If activated the CDS timing can be configured through the internal DLL. The DLL delay is locked to the external master clock.
- Offset correction and programmable gain functions can be provided to the signal. The gain function can be bypassed.
- It is possible to activate as many channels as needed from 1 to 16.

3.2 Temperature Measurements

The ASIC has the ability to measure two external and up to 16 internal temperatures. The selection of the temperature measurement is accomplished through a configuration register.

4 Power Supplies

The recommended external power supply connections of the ASIC are shown in Fig. 2.

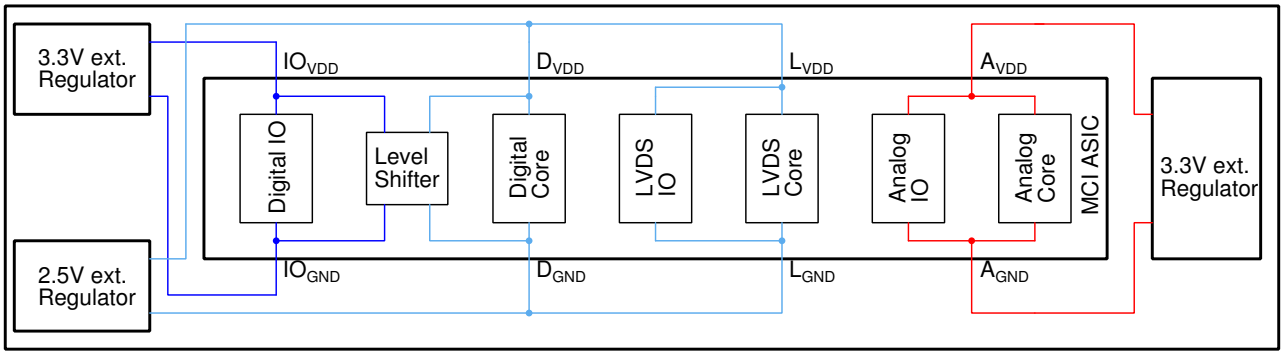


Figure 2: Power Supply Connections for the MCI ASIC.

5 Absolute Maximum Ratings

Parameter		Symbol	Min	Typ	Max	Units
AVDD Supply Voltage		AVDD_max	-0.3		5.0	V
IOVDD Supply Voltage		IOVDD_max	-0.3		5.0	V
DVDD Supply Voltage		DVDD_max	-0.3		5.0	V
LVDD Supply Voltage		LVDD_max	-0.3		5.0	V
Analog Input Voltage		VAi_max	-0.5		AVDD+0.5	V
Digital Input Voltage		VDi_max	-0.7		IOVDD+0.7	V
LVDS Input Voltage		VLi_max	-0.5		LVDD+0.5	V
ESD Rating	Human Body Model	HBM	2000			V
	Machine Model	MM	200			V
	Charged Device Model	CDM	500			V
Storage Temperature		Tstg	-55	25	+150	°C

Note 1: The analog inputs are protected as shown below. Analog input voltage magnitudes beyond the supply rails will not damage the device, provided the current is limited per Note 2 under the absolute maximum ratings. However, input errors will be generated if the input goes above AVDD and below AGND.

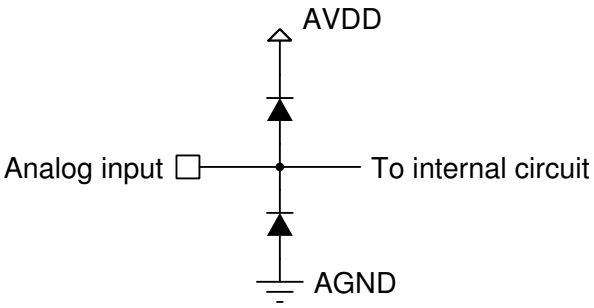


Figure 3: Analog input protection diodes.

Note 2: When the analog input voltage (VAi) at any pin exceeds the power supplies (VAi < AGND-0.5V or VAi > AVDD+0.5V), the current at that pin should be limited to 40 mA each pin.

6 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Analog Supply Voltage	AVDD	2.97	3.3	3.63	V
Digital_IO and LVDS RCV Supply Voltage	IOVDD	2.97	3.3	3.63	V
Digital_CORE Supply Voltage	DVDD	2.25	2.5	2.75	V
LVDS DRV Supply Voltage	LVDD	2.25	2.5	2.75	V
Operating Temperature	Ta	-55	25	+125	°C

7 Electrical Characteristics

Typ Condition:

- AVDD = 3.3V, IOVDD = 3.3V, DVDD = 2.5V, LVDD = 2.5V
- Ta = 25 °C CL = 10 pF, FClk = 20 MHz

Min, Max Conditions:

- AVDD = 3.3V ± 10%, IOVDD = 3.3V ± 10%, DVDD = 2.5V ± 10%, LVDD = 2.5V ± 10%
- Ta = -55 to +125 °C, CL = 10 pF, FClk = 20 MHz

7.1 CMOS Digital Inputs DC Specifications

(Digital Input Pins: SCLK, MCLK, LCSEL, PDB, PDB_LVDS, SENB, SDI, CLPIN)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High level input voltage	VIH		1.569			V
Low level input voltage	VIL				1.048	V
High level input current	IIH	SDI, CLPIN, MCLK SCLK, LCSEL, PDB, PDB_LVDS SENB	60	82	1.0 100 1.0	uA uA uA
Low level input current	IIL	SDI, CLPIN, MCLK SCLK, LCSEL, PDB, PDB_LVDS SENB	-1.0 -1.0 -100	-82	-60	uA uA uA

(Digital Input Pin: RSTB)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High level input voltage	VIH		2.573			V
Low level input voltage	VIL				0.781	V
Hysteresis voltage	Vhys		1.112		1.534	V
High level input current	IIH		60	82	100	uA
Low level input current	IIL				1.0	uA

7.2 CMOS Digital Outputs DC Specifications

(Digital Output Pins: DTM0, DTM1, SDO)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
High level output voltage	VOH	IOH = 2 mA	0.8 x IOVDD (2.376)			V
Low level output voltage	VOL	IOL = 2 mA			0.2 x IOVDD (0.726)	V

7.3 LVDS Inputs DC Specifications

(LVDS Input Pins: LVMCLKP, LVMCLKN)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential input voltage	VID	RL = 100 Ω (1)	100	350		mV
Input common mode voltage	VCM	RL = 100 Ω (1)	0.25	1.25	2.25	V

(1) 100 Ω input termination resistors are external components.

7.4 LVDS Outputs DC Specifications

(LVDS Output Pins: LVSCLKP/N, LVDOxxP/N, LVFRMP/N)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential output voltage	VOD	code = 0 x 0,	230	250	270	mV
Input common mode voltage	VCM	RL = 100 Ω	1.22	1.25	1.26	V
Differential output voltage	VOD	code = 0 x 1,	280	300	320	mV
Input common mode voltage	VCM	RL = 100 Ω	1.22	1.25	1.26	V
Differential output voltage	VOD	code = 0 x 2,	330	350	370	mV
Input common mode voltage	VCM	RL = 100 Ω	1.22	1.25	1.26	V
Differential output voltage	VOD	code = 0 x 3,	380	400	420	mV
Input common mode voltage	VCM	RL = 100 Ω	1.22	1.25	2.6	V

7.5 Power Supply Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
TSMC						
AVDD supply Current	IA				310	mA
AVDD supply Current Powerdown	IAPD				17	mA
IOVDD supply Current	IDIO				6	mA
IIOVDD supply Current Powerdown	IDIOPD				0.1	mA
DVDD supply Current	ID				34	mA
DVDD supply Current Powerdown	IDPD				29	mA
LVDD supply Current	IL				78.5	mA
LVDD supply Current Powerdown	ILPD				0.1	mA
Average power Dissipation	PWR				1.31	W
Power supply Rejection Ratio	PSRR	PGA=1x at 1 MHz			-44	dB

7.6 Analog Inputs Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input signal voltage (1)	VIN			2.5		Vpp
Reset noise	VRESET		500			mV

(1) When an input signal is the maximum at 2.5 V, the voltage of AVDD and IOVDD makes 3.135 V the minimum. ADC Data might overflow by a gain setting of PGA.

7.7 Clamp Circuit Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
VCLP DAC resolution				4		Bits
VCLP DAC max Voltage	VCLP max	AVDD = 3.3V		3.2		V
VCLP DAC min Voltage	VCLP min	AVDD = 3.3V		1.7		V
Pull-in time	Tclp	MCLK = 20 MHz CLAMP x Pulse Width = 3.9 ns			3	ms
Voltage Error (1)	Vclp_err				1	%

(1) The difference between convergent voltage and VCLP voltage due to Clamp action.

7.8 CDS Circuit Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CDS Bypass				Yes		Bits
CLAMP x Pulse Width	Tw_clp	MCLK = 20 MHz	3.9			ns
SAMPLE x Pulse width	Tw_spl	MCLK = 20 MHz	3.9			ns

7.9 Offset DAC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution				8		Bits
Offset adjustment range referred to AFE input (PGA gain = 1x)		Minimum DAC code = 0x00		-1000 (-1002.378)		mV
		Maximum DAC code = 0xFF		+200 (+197.652)		mV
Differential Non-Linearity	DNL		-0.5		+0.5	LSB
Integral Non-Linearity	INL		-2.0		+2.0	LSB

7.10 Test DAC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution				3		Bits
PGA Input Voltage range		Minimum DAC code = 0x00			0	V
		Maximum DAC code = 0x07				2.5V
ADC Output Code (PGA gain = 1.x)		Minimum DAC code = 0x00		0		LSB
		Maximum DAC code = 0x07		4095		LSB

Parameter set of Test DAC is available independently by each CH. DNL and INL don't define it.

7.11 PGA Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gain resolution				8		Bits
Maximum gain			25.0	26.0	27.0	dB
Minimum gain			-0.8	0	0.8	dB
PGA Bypass				Yes		

Parameter set of PGA is available independently for each CH.

7.12 ADC Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Gain resolution				12		Bits
Input voltage range				2.5		V
Over range output code					4095	
Under range output code			0			
Conversion rate			3		20	Msps

7.13 DLL Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Resolution				64		Step
Delay step		FMClk: 3 to 20 MHz		1/(64xFMClk)		ns
Lockup time		FMClk = 20 MHz			100	us
Jitter		FMClk = 20 MHz			50	ps

7.14 Timing Generator Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
CLAMP Pulse width	Tw_clp	FMClk: 3 to 20 MHz	5/(64xFMClk) (3.9)			ns
SAMPLE Pulse width	Tw_spl	FMClk: 3 to 20 MHz	5/(64xFMClk) (3.9)			ns

7.15 PLL Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output frequency		FMClk = 20 MHz			240	MHz
Lockup time		FMClk = 20 MHz			100	us
Jitter		FMClk = 20 MHz			40	ps

7.16 Full Channel Performance Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Differential Non-Linearity	DNL	PGA = 1x	-0.5		0.5	LSB
Integral Non-Linearity	INL	PGA = 1x	-2.0		2.0	LSB
Channel to channel Crosstalk					-70	dB
Peak Signal to Noise Ratio	PSNR	PGA = 10x	70			dB
Effective Number Of Bits	ENOB	PGA = 10x	9.84			Bits

7.17 Power on Reset Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Reset Voltage (DVDD_CORE)	Vpor		1.45	1.80	2.15	V
Comparator Hysteresis	Vhys		0.04	0.1	0.2	V

7.18 Temperature Measurements Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
ADC resolution				12		Bits
Number of connections of Ext. sensors				2		CHs
Measurement accuracy					0.1	°C

8 AC Timing Specifications

8.1 Input Clock Timing Specifications

(Input Clock Pins: VMCLKP, LVMCLKN, MCLK)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input clock frequency	FMClk	ADC rate clock	3		20	MHz
Input clock duty cycle	Tdc		40 / 60	50 / 50	60 / 40	%

8.2 Full Channel Latency Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Pipeline latency	Tlat			4		MClk

8.3 LVDS Outputs Timing Specifications

The timing diagrams for the Serialized 16 CH ADC data, clock and Frame pulse LVDS Outputs are shown in Figs 4.

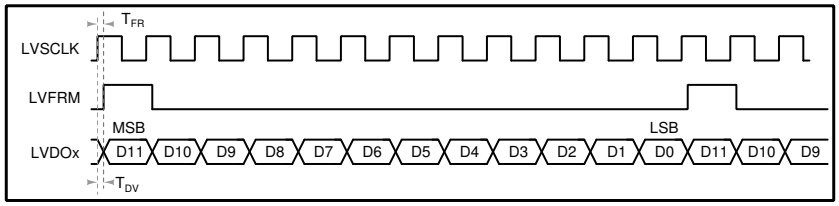


Figure 4: LVDS Outputs timing diagrams.

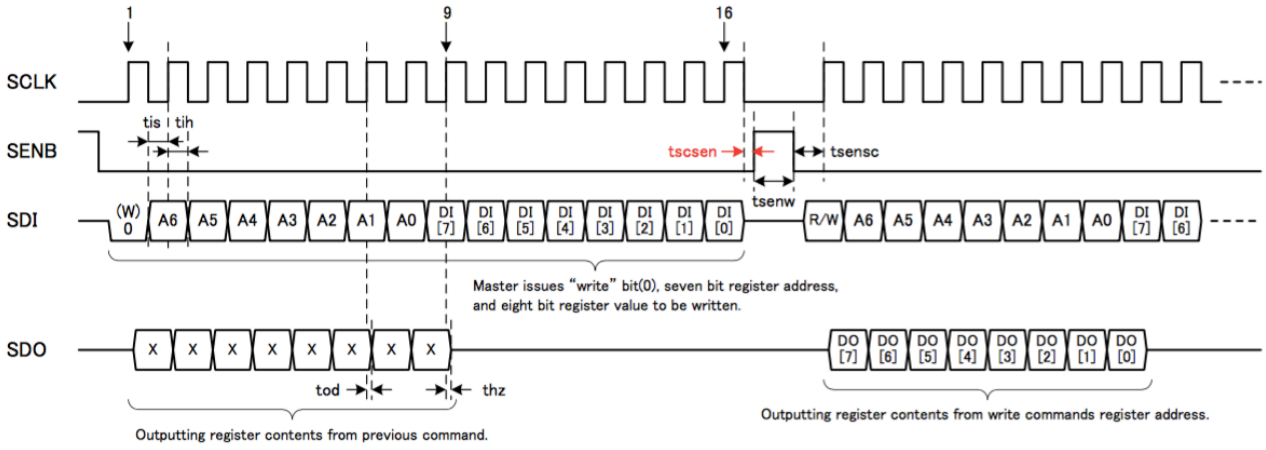
The timing parameters are shown in the following table.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
LVSCLK rising to	Tfr	Tj:-55 to +125 °C	0.8		2.2	ns
LVSCLK rising to	Tdv	Tj:-55 to +125 °C	0.9		2.2	ns
Clock Duty Cycle	Tdc_{SCLK}		44	50	56	%

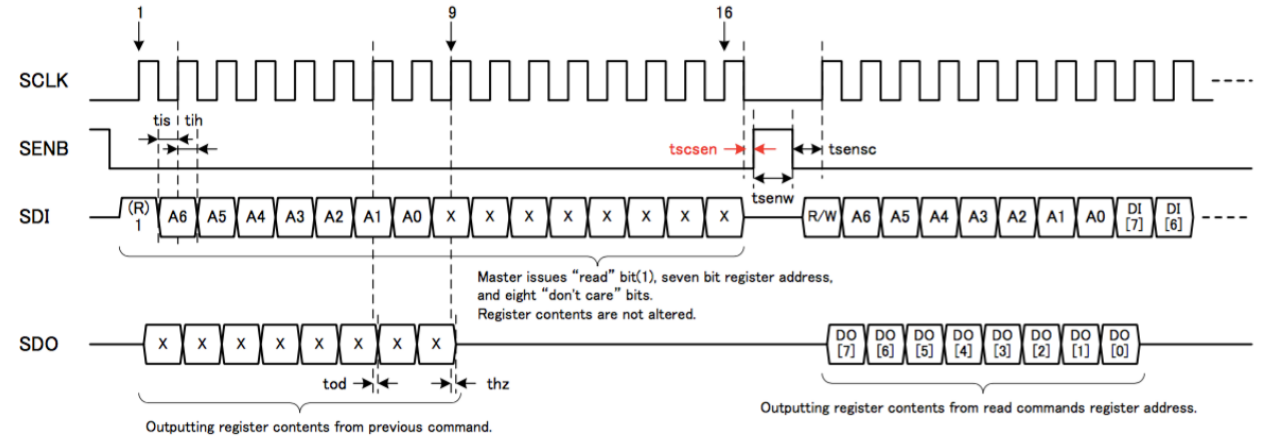
(LVDS Output Pins: LVSCLKP/N, LVDOxxP/N, LVFRMP/N)

8.4 Serial Interface Timing Specifications

The timing diagrams for the SPI Write and Read functions are shown in Figs 5.



(a) Write



(b) Read

Figure 5: Timing diagrams of the SPI interface.

The timing parameters are shown in the following table.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
SCLK frequency	fsclk			1	20	MHz
SCLK duty cycle	Tsdc		40 / 60	50 / 50	60 / 40	%
Input hold time	Tih		2.0	2.5		ns
Input setup time	Tis		1.0	2.5		ns
SCLK start time after SENB low	tsensc		1.0	1.5		ns
SENB high after last SCLK falling edge	tscsen		2.0	2.5		ns
SENB pulse width	tsenw		6.0	8.0		ns
Output delay time	tod			10.54	11.6	ns
Data output to high Z	thz			1.2	1.23	Tsclk

(Serial Interface Pins: SCLK, SENB, SDI, SDO)

8.5 Digital Timing Monitor Reference Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise time	tr_dtm				3.2	ns
Fall time	tf_dtm				3.2	ns

9 Register Map

The ASIC can be programmed through a serial interface. The programming is accomplished through a set of internal registers. The address map and the description of the registers is shown in the table below. Power-on-Reset sets the Baseline value.

Address (Hex)	Register Title	Baseline	Bits	Function	Init. Status
00	Analog Power Down	0000 0000	7	Analog Power Down 8	Power Down
			6	Analog Power Down 7	Power Down
			5	Analog Power Down 6	Power Down
			4	Analog Power Down 5	Power Down
			3	Analog Power Down 4	Power Down
			2	Analog Power Down 3	Power Down
			1	Analog Power Down 2	Power Down
			0	Analog Power Down 1	Power Down
01	Analog Power Down	0000 0000	7	Analog Power Down 16	Power Down
			6	Analog Power Down 15	Power Down
			5	Analog Power Down 14	Power Down
			4	Analog Power Down 13	Power Down
			3	Analog Power Down 12	Power Down
			2	Analog Power Down 11	Power Down
			1	Analog Power Down 10	Power Down
			0	Analog Power Down 9	Power Down
02	ByPass and LVDS Control	0000 0010	[7:4]	Not Used	N/A
			3	CDS ByPass	OFF
			2	PGA ByPass	OFF
			[1:0]	LVDS VOD	350mV Vpp
03	DLL PLL Control	0000 0011	[7:4]	Not Used	N/A
			3	DLL Power Down	Power Down
			2	PLL Power Down	Power Down
			1	DLL Reset	Normal Operation
			0	PLL Reset	Normal Operation
04	Offset DAC 1	1101 0101	[7:0]	Offset DAC 1	0
05	PGA Gain 1	0000 0000	[7:0]	PGA Gain 1	-6dB
06	Test DAC 1/Test Pattern 1	0000 0000	7	Not Used	N/A
			[6:4]	Test DAC 1	0
			[3:0]	Test Pattern[11:8]1	0
07	Test Pattern 1	0000 0000	[7:0]	Test Pattern[7:0]1	0
08	Offset DAC 2	1101 0101	[7:0]	Offset DAC 2	0
09	PGA Gain 2	0000 0000	[7:0]	PGA Gain 2	-6dB
0A	Test DAC 2/Test Pattern 2	0000 0000	7	Not Used	N/A
			[6:4]	Test DAC 2	0
			[3:0]	Test Pattern[11:8]2	0
0B	Test Pattern 2	0000 0000	[7:0]	Test Pattern[7:0]2	0
.	.	.	.	.	.
.	.	.	.	.	.
.	.	.	.	.	.
40	Offset DAC 16	1101 0101	[7:0]	Offset DAC 16	0
41	PGA Gain 16	0000 0000	[7:0]	PGA Gain 16	-6dB
42	Test DAC 16/Test Pattern 16	0000 0000	7	Not Used	N/A
			[6:4]	Test DAC 16	0
			[3:0]	Test Pattern[11:8]16	0
43	Test Pattern 16	0000 0000	[7:0]	Test Pattern[7:0]16	0
44	VCLP DAC	0000 1100	[7:4]	Not used	N/A
			[3:0]	VCLP DAC	2.9
45	Not used	0000 0000	[7:0]	Not used	
46	Not used	0000 0000	[7:0]	Not used	
47	Not used	0000 0000	[7:0]	Not used	
48	Clamp Start	0000 0100	[7:6]	Not Used	
			[5:0]	Clamp Start	4/64

Continued on next page

– continued from previous page

Address (Hex)	Register Title	Baseline	Bits	Function	Init. Status
49	Clamp End	0001 1000	[7:6] [5:0]	Not Used Clamp End	 24/64
4A	Sample Start	0010 0101	[7:6] [5:0]	Not Used Sample Start	 37/64
4B	Sample End	0011 1010	[7:6] [5:0]	Not Used Sample End	 58/64
4C	Test Enable	0000 0000	[7:4] [3] [2] [1] [0]	Not Used Test DAC Enable Test PG Enable DTM1 Enable DTM0 Enable	 0 0 0 0
4D	Temp. Measure Control	0000 0000	[7:3] [2] [1:0]	Not Used Int. Temp. Meas. Control Ext. Sensor Connection	 Disable CCD, CCD
4E	Temp. Meas. Data T0	0000 0000	[7:4] [3:0]	Not Used T0 4 MSBs	
4F	Temp. Meas. Data T0	0000 0000	[7:0]	T0 8 LSBs	
50	Temp. Meas. Data T1	0000 0000	[7:4] [3:0]	Not Used T1 4 MSBs	
51	Temp. Meas. T1	0000 0000	[7:0]	T1 8 LSBs	
52	Temp. Meas. Data iTS0	0000 0000	[7:4] [3:0]	Not Used iTS0 4 MSBs	
53	Temp. Meas. Data iTS0	0000 0000	[7:0]	iTS0 8 LSBs	
54	Temp. Meas. Data iTS1	0000 0000	[7:4] [3:0]	Not Used iTS1 4 MSBs	
55	Temp. Meas. Data iTS1	0000 0000	[7:0]	iTS1 8 LSBs	
. . .	. . .	. . .	. . .	. . .	. . .
70	Temp. Meas. Data iTS15	0000 0000	[7:4] [3:0]	Not Used iTS15 4 MSBs	
71	Temp. Meas. Data iTS15	0000 0000	[7:0]	iTS15 8 LSBs	

10 Communication Interfaces

An SPI serial interface is implemented into the MCI ASIC to cover its communication needs (temperature measurements data transfers, control/configuration and monitoring).

11 Clocking Scheme

The clock diagram of the MCI ASIC is shown in Fig. 6.
The ADC master clock is delivered to the ASIC via

- either a CMOS input pin or,
- a differential LVDS pin with an external resistor of 100 Ω.

The selection is performed through pin *LCSEL*. The default configuration is the differential clock input. The resulting internal clock (*i_MCLK*) is fed to the rest of the ASIC. The following units are used:

- A DLL unit to produce the reference and video level sampling pulses.
- A PLL unit to produce the serial LVDS clock.

The SPI clock is delivered through pin *SCLK*.

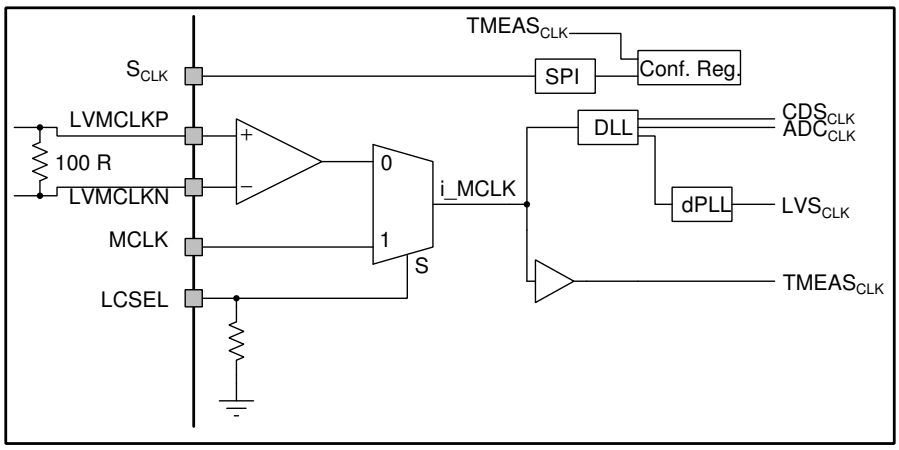


Figure 6: Clock diagram of the MCI ASIC.

12 Theory of Operation

12.1 CDS function on input signal

For CCD and CMOS sensor signals the input is processed by the CDS unit as shown in FIg. 7.

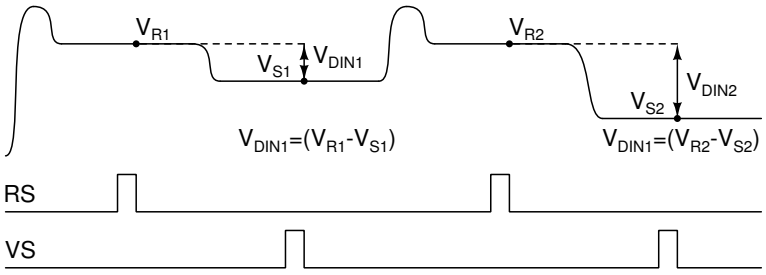


Figure 7: Input waveform and CDS output.

The output voltage of the CDS is equal to

$$V_{DIN} = V_R - V_S \tag{1}$$

12.2 Transfer Function

The transfer function of the ASIC with respect to the CDS output signal V_{DIN} is shown in Fig. 8.

12.3 Clamping

The equivalent circuit for the clamp unit is shown in Fig. 9.

12.4 Power Down Modes

The ASIC implements a power down mode. The power down mode is controlled by the SPI and pins PDB and PDB$_{LVDS}$. Upon power up or reset the ASIC enters power down mode.

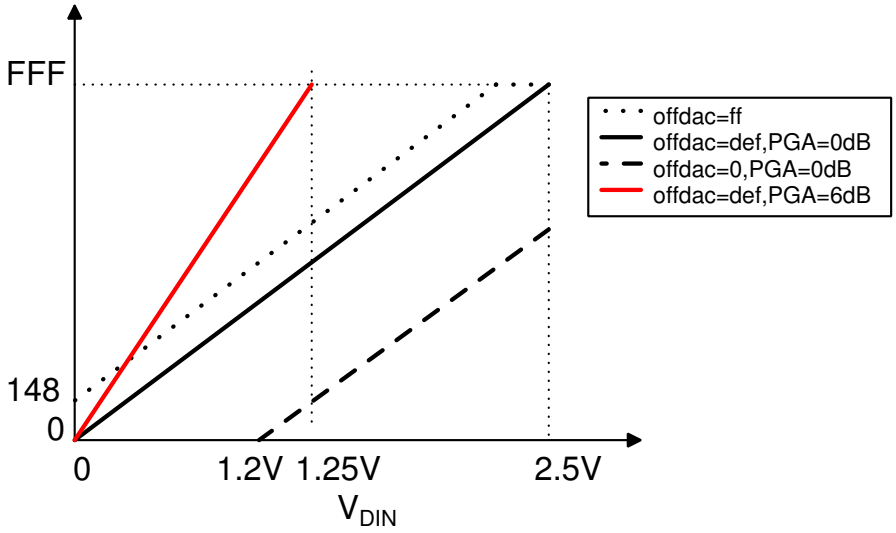


Figure 8: Transfer function of the MCI ASIC channel versus PGA and Offset DAC settings.

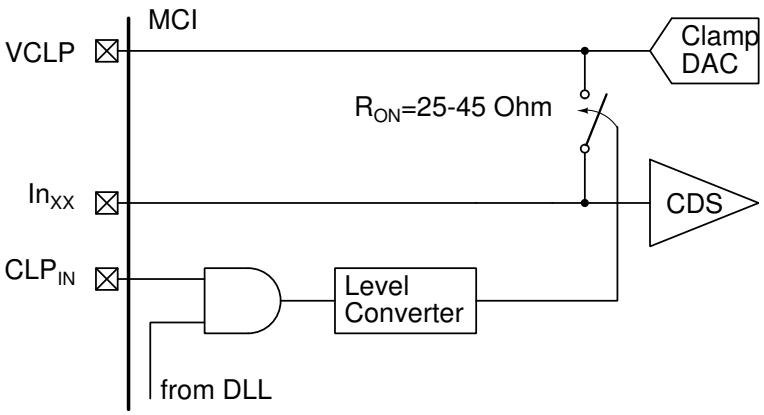


Figure 9: Equivalent circuit of the clamp logic.

12.4.1 Power Down Mode Operations

During Power down mode the ASIC can:

- Communicate through the SPI interface and
- measure temperatures.

12.4.2 ASIC getting out of the power down mode

The ASIC gets out of the power down mode by SPI commands and by pulling high pins PDB and PDB_{LVDS}. The equivalent circuit is shown in Fig. 10.

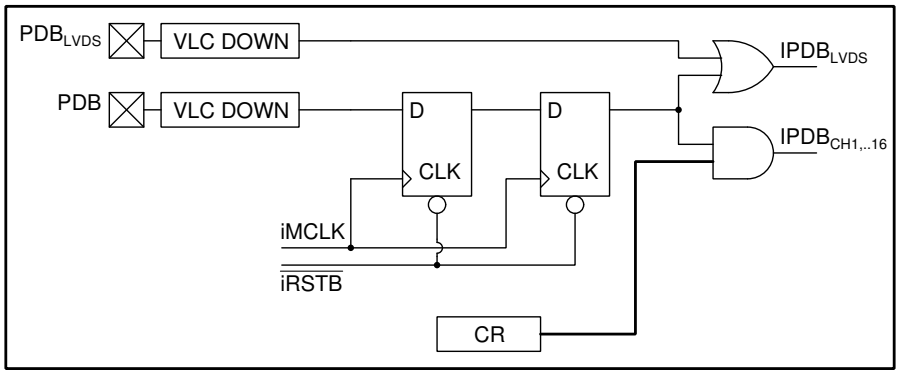


Figure 10: PDB Equivalent circuit.

12.5 Temperature Measurement

The temperature measurement system is shown in Fig. 11.
It can measure :

1. 2 external sensors (either PT or NTC, or direct voltages) and
2. 16 internal PTAT sensors.

The topology of the internal PTAT sensors is shown in Fig. 11. They are located inside each channel between the PGA and channel ADC units. Thus, they can be used to correct for temperature drift on the PGA and the channel ADC. The user can enable or disable the internal temperature measurement unit through an SPI command.
The equivalent circuit for interfacing voltage or resistor based sensors on inputs T0 and T1 is shown in Fig. 12. In the lest side the equivalent circuit for interfacing external voltage sensors is shown. Switch M1 is open and thus the user can apply directly voltages to nodes T0 and T1. These voltages are sampled by the temperature measurement 12 bit ADC. On the right side the equivalent circuit for interfacing external resistor sensors is shown. The switch M1 is allowed to be controlled by the temperature measurement state machine. Thus the current source output current is fed to the resistive sensor. The voltage developed on the sensor is then quantized by the ADC. The sensor current is defined as

$$I_{SENSOR} = \frac{0.2 \times V_{REFIN}}{R_C} \tag{2}$$

where R_C is an external low temperature coefficient resistor.

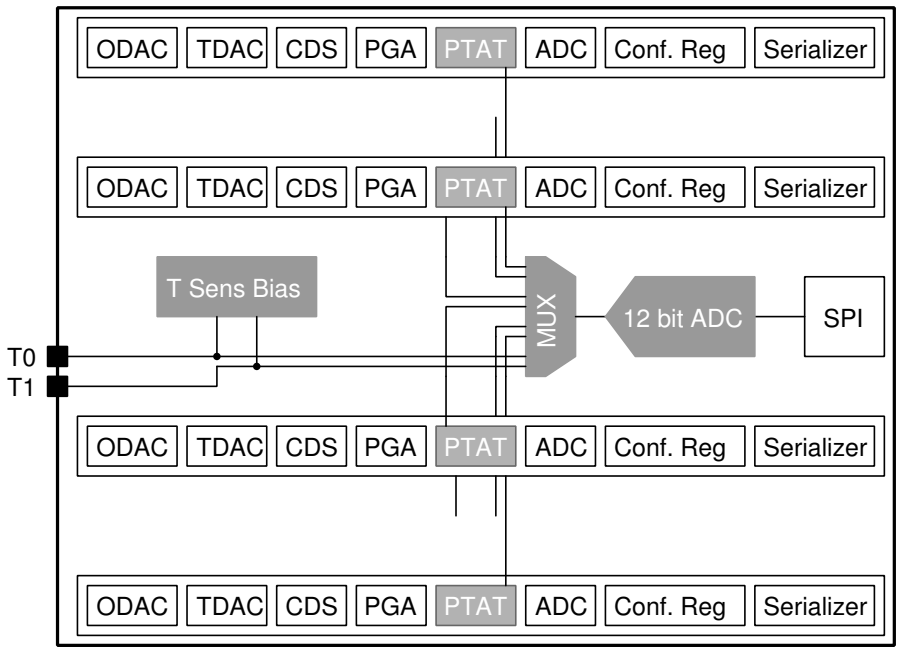


Figure 11: MCI ASIC temperature measurement circuit.

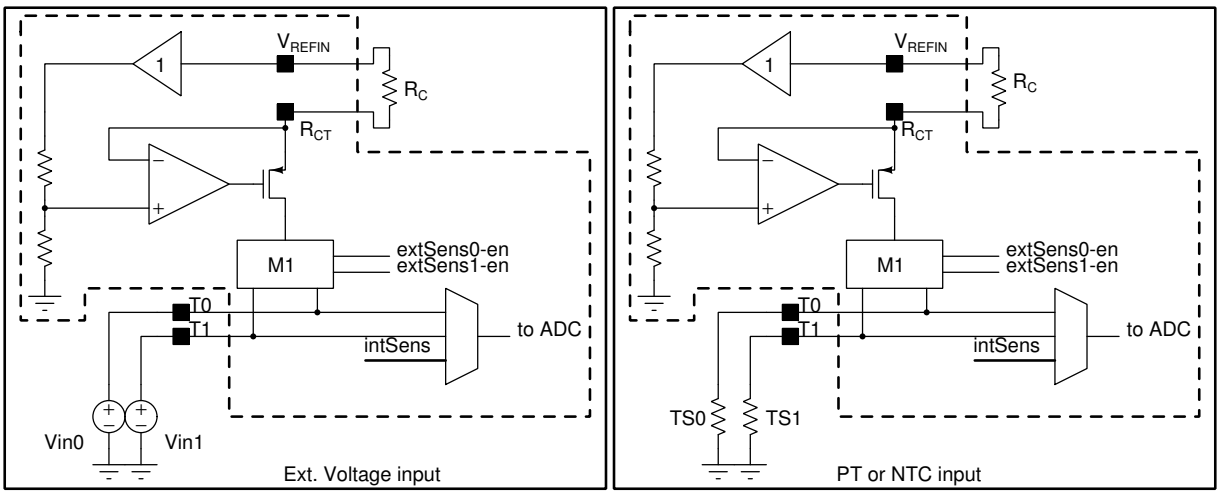


Figure 12: Simplified circuit for interfacing voltage or resistor based sensors

13 Performance

13.1 Channel performance

The channel non linearity is shown in Fig. 13. The non linearity is calculated as

$$NL = OC_{REAL} - OC_{IDEAL} = OC_{REAL} - \frac{V_R - V_S}{V_{REF}} \times 4095 \tag{3}$$

Non linearity plots for all channels are presented.

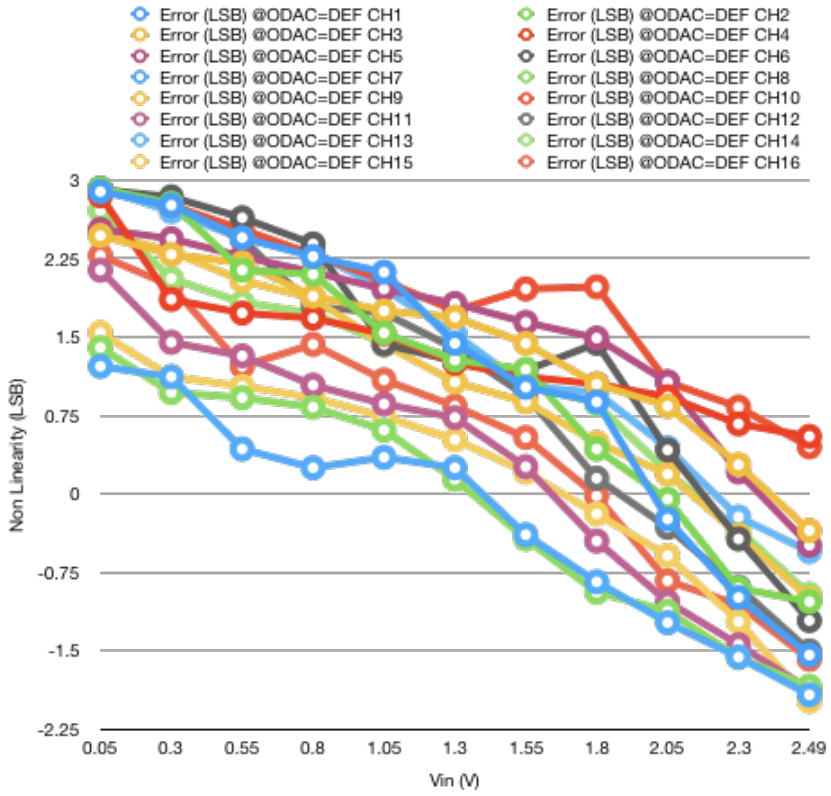


Figure 13: Typical Non Linearity of the MCI Device

The channel cross talk is shown in Fig. 14.

13.2 Temperature Measurement ADC

The non linearity of the temperature measurement ADC is shown in Fig. 15.

13.3 Internal Reference Temperature performance

Typical internal reference temperature performance is shown in Fig. 16.

14 Radiation Performance

14.1 TID

The MCI ASIC maintains its performance characteristics up to a TID level of at least 300 KRad (TBC).

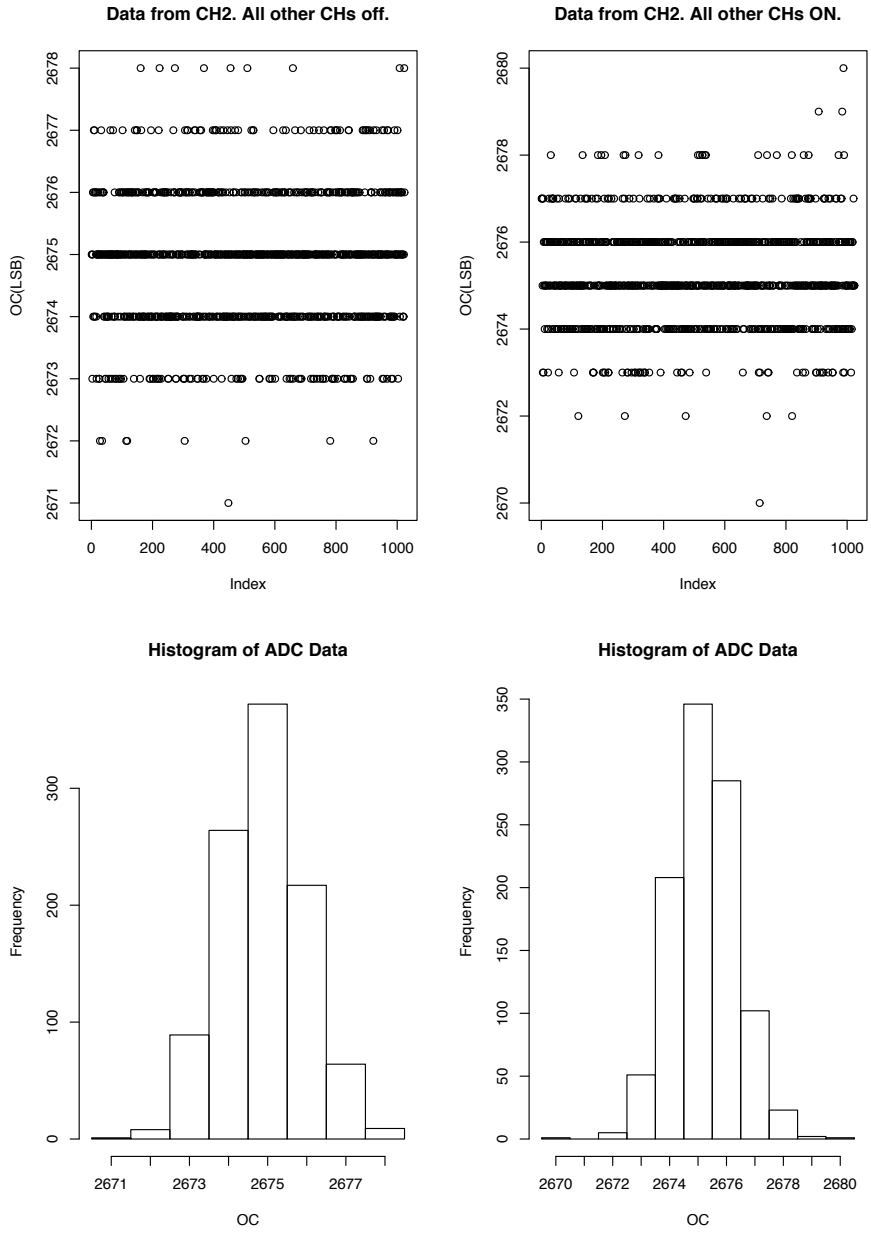


Figure 14: Output code and histogram for data on CH2. with all other channels off and on.

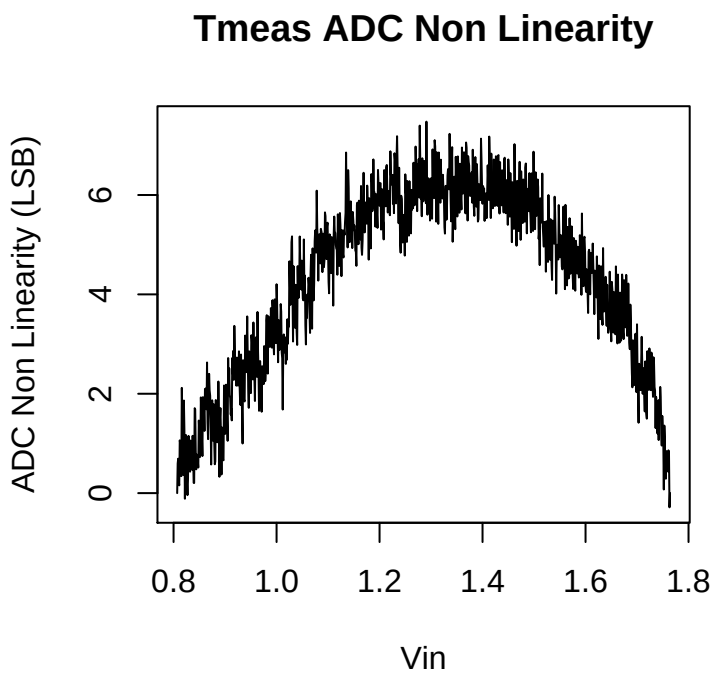


Figure 15: Non Linearity of the temperature measurement ADC.

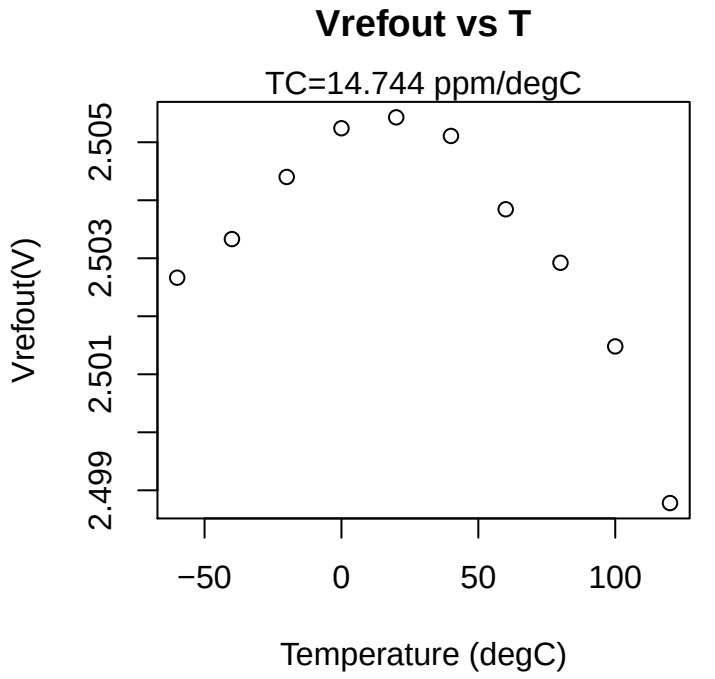


Figure 16: Typical temperature performance of the voltage reference.

14.2 SEE

The MCI ASIC has an SEE (SEU, SEL, SET and SEFI) LET threshold of at least 64 MeV/mg/cm^2 (TBC).

15 Mechanical Parameters

15.1 Package Physical Dimensions

The EM MCI ASIC is packaged in a 120 pin PGA package.
The physical parameters of the package are shown in Fig. 17.

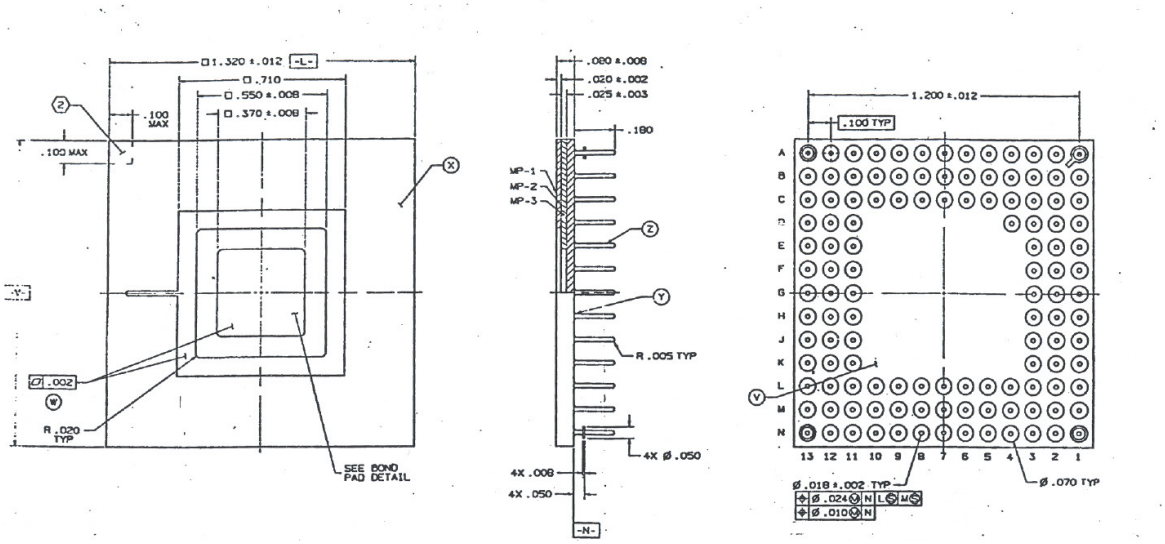


Figure 17: EM MCI ASIC Package Drawing.

The FM MCI ASIC will be packaged in a custom 100 pin CQFP package designed and manufactured by Kyocera. The physical parameters of the FM package are shown in Fig. 18.

15.1.1 Lid Grounding

The lid of the CQFP package will be electrically connected to the ground.

15.2 Bare Die Dimensions

The size of the bare die is 8.15 mm x 8.15 mm.

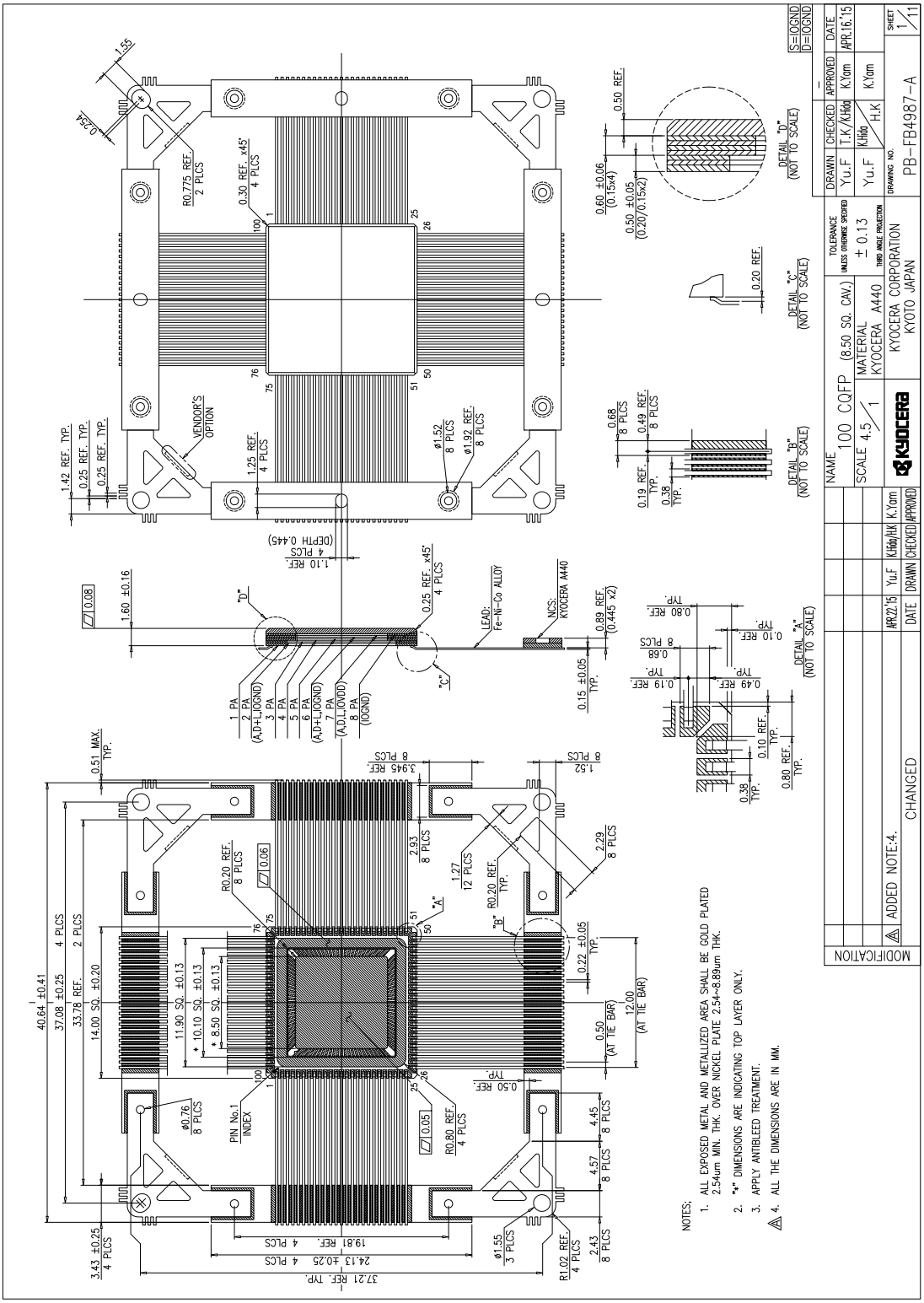


Figure 18: MCI ASIC Package Drawing.

16 Pins List

Table 28: Terminal connections of the CQFP packaged MCI device.

Lead No. on PGA 120	Name	I/O	Type	Int. Res. Conn.	Description
1	AVDD		P		Analog power supply
2	AVDD		P		Analog power supply
3	AGND		G		Analog ground
4	AGND		G		Analog ground
5	In1	I	A		CCD signal input 1
6	In2	I	A		CCD signal input 2
7	In3	I	A		CCD signal input 3
8	In4	I	A		CCD signal input 4
9	In5	I	A		CCD signal input 5
10	In6	I	A		CCD signal input 6
11	In7	I	A		CCD signal input 7
12	In8	I	A		CCD signal input 8
13	AVDD		P		Analog power supply
14	AVDD		P		Analog power supply
15	AGND		G		Analog ground
16	In9	I	A		CCD signal input 9
17	In10	I	A		CCD signal input 10
18	In11	I	A		CCD signal input 11
19	In12	I	A		CCD signal input 12
20	In13	I	A		CCD signal input 13
21	In14	I	A		CCD signal input 14
22	In15	I	A		CCD signal input 15
23	In16	I	A		CCD signal input 16
24	AVDD		P		Analog power supply
25	AVDD		P		Analog power supply
26	AGND		G		Analog ground
27	AGND		G		Analog ground
28	T0	I	A		Connect either voltage or the temperature sensor
29	T1	I	A		Connect either voltage or the temperature sensor
30	RCT	I	A		Connect low TC resistor from this pin to VREFIN to define the temperature sensor current.
31	TAC1	I	A		Connect 2.2nF capacitor to TAC2.
32	TAC2	I	A		
33	AVDD		P		Analog power supply
34	AGND		G		Analog ground
35	VRTRM0	I	A		Voltage reference trim pad
36	VRTRM1	I	A		Voltage reference trim pad
37	VRefOut	O	A		Voltage reference output
38	VRefIn	I	A		Connect to Vrefout
39	Test	I	D		Active-high test control pin
40	AVDD		P		Analog power supply
41	AGND		G		Analog ground
42	AGND		G		Analog ground
43	PDB_LVDS	I	D	Pd	LVDS Power down control
44	PDB	I	D	Pd	Power down control
45	RSRB	I	D	Pd	External reset
46	LCSEL	I	D	Pd	LVDS/CMOS selection of Main clock input
47	DVDD		P		Digital CORE power supply
48	DVDD		P		Digital CORE power supply
49	DGND		G		Digital CORE ground

Cont. –

– Cont.					
Lead No. on PGA 120	**Name**	**I/O**	**Type**	**Int. Res. Conn.**	**Description**
50	DGND		G		Digital CORE ground
51	LVDD		G		LVDS power supply
52	LGND		G		LVDS ground
53	LVDO16N	O	D		LVDS data output 16 negative
54	LVDO16P	O	D		LVDS data output 16 positive
55	LVDO15N	O	D		LVDS data output 15 negative
56	LVDO15P	O	D		LVDS data output 15 positive
57	LVDO14N	O	D		LVDS data output 14 negative
58	LVDO14P	O	D		LVDS data output 14 positive
59	LVDO13N	O	D		LVDS data output 13 negative
60	LVDO13P	O	D		LVDS data output 13 positive
64	LVDO12N	O	D		LVDS data output 12 negative
65	LVDO12P	O	D		LVDS data output 12 positive
66	LVDO11N	O	D		LVDS data output 11 negative
67	LVDO11P	O	D		LVDS data output 11 positive
68	LVDO10N	O	D		LVDS data output 10 negative
69	LVDO10P	O	D		LVDS data output 10 positive
70	LVDO9N	O	D		LVDS data output 9 negative
71	LVDO9P	O	D		LVDS data output 9 positive
72	LVSCLKN	O	D		LVDS clock output negative
73	LVSCLKP	O	D		LVDS clock output positive
74	LVDD		P		LVDS power supply
75	LGND		G		LVDS ground
76	LVMCLKN	I	D		LVDS Main clock input Negative
77	LVMCLKP	I	D		LVDS Main clock input Positive
78	MCLK	I	D		CMOS Main clock input
79	LVDO8N	O	D		LVDS data output 8 negative
80	LVDO8P	O	D		LVDS data output 8 positive
81	LVDO7N	O	D		LVDS data output 7 negative
82	LVDO7P	O	D		LVDS data output 7 positive
83	LVDO6N	O	D		LVDS data output 6 negative
84	LVDO6P	O	D		LVDS data output 6 positive
85	LVDO5N	O	D		LVDS data output 5 negative
86	LVDO5P	O	D		LVDS data output 5 positive
87	LVDO4N	O	D		LVDS data output 4 negative
88	LVDO4P	O	D		LVDS data output 4 positive
89	SEUF	O	D		SEU indicator flag output
91	LVDO3N	O	D		LVDS data output 3 negative
92	LVDO3P	O	D		LVDS data output 3 positive
93	LVDO2N	O	D		LVDS data output 2 negative
94	LVDO2P	O	D		LVDS data output 2 positive
95	LVDO1N	O	D		LVDS data output 1 negative
96	LVDO1P	O	D		LVDS data output 1 positive
97	LVFRMN	O	D		LVDS frame output negative
98	LVFRMP	O	D		LVDS frame output positive
99	LGND		G		LVDS ground
100	LGND		G		LVDS ground
101	LVDD		P		LVDS power supply
102	LVDD		P		LVDS power supply
103	IOGND		G		Digital IO ground
104	IOVDD		P		Digital IO power supply
105	SDO	O	D		Data output for serial interfaces
106	SENB	I	D	Pu	Active-low chip enable for serial interface
107	SCLK	I	D	Pd	Clock input for serial interfaces
108	SDI	I	D		Data input for serial interfaces
109	DGND		G		Digital CORE ground
110	DGND		G		Digital CORE ground
					Cont. –

– Cont.					
Lead No. on PGA 120	**Name**	**I/O**	**Type**	**Int. Res. Conn.**	**Description**
111	DVDD		P		Digital CORE power supply
112	DTM0	O	D		Digital timing monitor 0
113	DTM1	O	D		Digital timing monitor 1
114	IOGND		G		Digital IO ground
115	IOVDD		P		Digital IO power supply
116	CLPIN	I	D		Input clamp signal
117	P2	I	D		Active-low test pin
118	P1	IO	D		Active-low input test pin when in test mode. Flag output in nominal operation mode.
119	P0	I	D		Active-low test pin
120	VCLP	I	A		Clamping voltage monitor 0.1 uF connection

where,

- I = Input, O = Output, IO = Bi-directional
- A = Analog, D = Digital, P = Power, G = Ground
- Pu = Pull up with internal resistor, Pd = Pull down with internal resistor