ETM ASIC
Data Sheet

Doc ID	:	D-SA-ETM-2.3.2-EDS
Version	:	4
Revision	:	D
Date	:	September 16, 2015
Classification	:	For public release

SPACE-ASICS SA
Didotou 9
Athens, 10680 Greece
Tel:+30-210-32569931
Fax: +30-210-3256995
Mail: info@space-asics.gr
Web: www.space-asics.gr

Page intentionally left blank

REVISION HISTORY

Revision	Date	Comments
Version 1A	January 10, 2009	CDR level.
		As agreed at CDR level.
Version 2A	January 31, 2011	Updated with EM DVR information.
		As delivered at EM DVR level.
Version 2B	March 31, 2011	An Application Note for proper CSC/DC setup and configuration has been included (see section 16).
Version 2C	July 15 2011	As agreed with ESA at EM DVR level.
Version 3A	May 28, 2012	Updated with FM information.
		Updated with information regarding variable transmission rates of the PW interface. See section 5.1.1.
		Updated with information regarding the operating current. See section 10.6.
		Digital operating current versus clock frequency updated. See section 10.7.
		Package information updated so as to include FM ETM package options. See section 12.1.
		As delivered at FM DVR level.
Version 3B	September 14, 2012	Updated with information regarding cross-strapping of analog and digital inputs. See section 14. This update partially covers PDR-AI-2.
		Differential and single ended voltage sampling capability description inserted. See section 3.4.
		Temperature measurement capability description inserted. See section 3.5.
		Digital input sampling capability description inserted. See section 3.7.
		As delivered to potential customers after AMICSA 2012.
Version 3C	December 7, 2012	Updated version that closes all action items related to this document during the entire project.
		Updated with methods for the user to verify the POR functionality, in response to DVR1-AI-9. See section 7.
		Table 30 in section 10.9 was updated with information regarding power supply ripple requirements in response to DVR1-AI-26.
		Table 30 in section 10.9 was updated with information regarding internal Voltage Reference min and max values in response to DVR1-AI-27.
		Digital Sampler threshold setting through a bias resistor and SET susceptibility information were inserted in response to DVR1-AI-56. See section 10.5.1.
		In addition, information on how to extend the Digital Sampler input range was inserted in response to DVR1-AI-56. See section 10.5.2.
		Information on how to control the internal clock oscillator output frequency, through pad *C_CLK*, was added in response to PTR April 7 teleconf. AI-4. See section 6.2.
		Information on how to connect static digital input pins was inserted in response to PTR April 15 teleconf. AI-4. See section 13.2.
		Updated with information regarding Voltage Reference performance and configurations. See section 10.2.
		Updated with information regarding the extension of the analog input range measurements. See section 10.3. This update partially covers PDR-AI-2 (complete coverage with update of version V3RB).
Version 3D	January 7, 2013	Updated with information regarding the expedited SDO messages. See section 5.2.3.
Version 3E	March 25, 2013	Updated with information regarding the voltage reference setting options. See section 3.6.
		Internal voltage reference performance further documented. See section 10.2.
		Digital sampler data shift out order corrected. See section 4.1.
		SEU threshold corrected to 32 MeV/mg/cm^2. See section 1.
		Information added regarding the handling of the device in a system while it is powered off. See section 7.3.
		Anomaly indication and TOS fields contents updated. See sections 4.4.2 and 4.4.1.
		Various typo corrections performed.
		As agreed at FM DVR level.

continued on next page –

continued from previous page

Revision	Date	Comments
Version 4A	March 25, 2013	Anomaly indication and TOS fields contents further updated. See sections 4.4.2 and 4.4.1
Version 4B	January 14, 2014	Lid grounding information added. See section 12.3.1.
		Table that describes how to operate the device in internal/external clock mode corrected. See table 18.
		Characteristics of output *ScSeqRun* updated. See section 3.10
		Information regarding the ETM Space Packet size updated. See section 4.2.
		Information regarding the two different clocks in RTU mode added. See section 6.3.
Version 4C	August 26, 2014	TID and SEE performance added. See section 11.
Version 4D	September 16, 2015	Pin list updated. See section 13.

APPLICABLE DOCUMENTS

D1 Space Packet Protocol, CCSDS Blue Book, CCSDS 133.0-B-1, September 2003.
D2 SCTMTC ASIC Users Manual, P-ASIC-NOT-00122-SE, Issue 12.
D3 Recommendations for CAN Bus in Spacecraft Onboard Applications, Draft 2.1, May 2005.
D4 CAN Specification, Version 2.0 BOSCH.
D5 Telemetry and telecommand packet utilization, ECSS-E-70-41A, Annex A.
D6 Spacecraft Discrete Interfaces, ECSS-E-ST-50-14C, July 2008.

Contents

List of Acronyms

ADC	Analog to Digital Converter
AFEND	Analog Front END
ASIC	Application Specific Integrated Circuit
ASMN	Analog Signal Monitor
BLMN	Bi-Level Monitor
CAN	Controller Area Network
CCSDS	Consultative Committee for Space Data Systems
COB-ID	Communication Object Identifier
DNL	Differential Non-Linearity
CSC/DC	CaSCaded/Daisy-Chain mode
DUTH/SRL	Demokritos University of Thrace/Space Research Laboratory
ECSS	European Cooperation for Space Standardisation
EM	Engineering Model
ESA	European Space Agency
ETM	Essential TeleMetry
INL	Integral Non-Linearity
LDUT	Large Data Unit Transfer
LET	Linear Energy Transfer
NMT	Network Management
NTC	Negative Temperature Coefficient
OD	Object Dictionary
PCB	Printed Circuit Board
POR	Power On Reset
PRT	Platinum Resistance Temperature sensor
PW	PacketWire
RTU	Remote Terminal Unit mode
SDO	Service Data Object
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
SP	Space Packet
STD	STanD alone mode
SYNC	Synchronisation Object
TC	Temperature Coefficient
TID	Total Ionizing Dose
TOS	Time of Origin Stamp
TSMN	Temperature Sensors Monitor
ZIF	Zero Insertion Force

Introduction

This document is the data sheet of the Essential Telemetry (ETM) support ASIC.
It presents information based on the FM design of ETM.
The ETM ASIC was developed by SPACE-ASICS & DUTH/SRL under ESA contract No. 20198/06/NL/GLC.

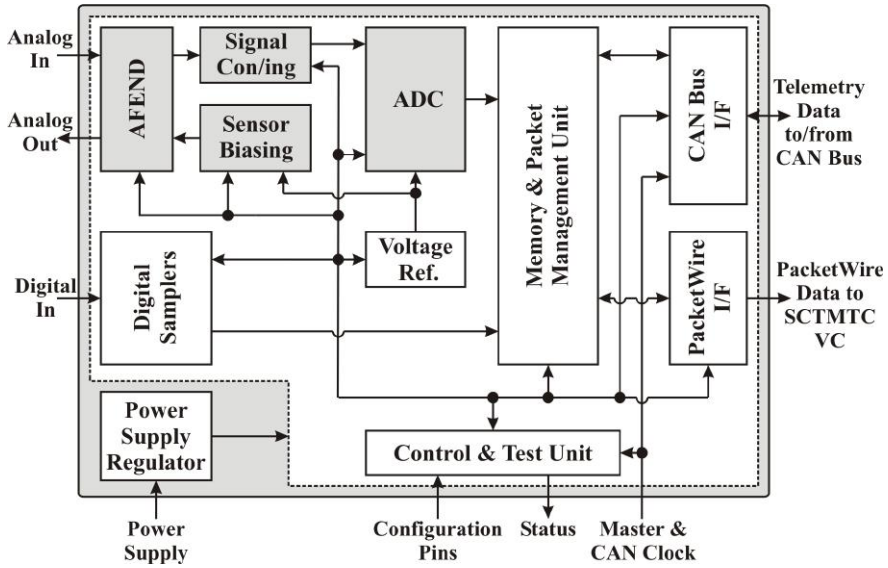
1 Functionality

The ETM-ASIC autonomously performs the following tasks as soon as power is supplied:

- Sequential scanning and sampling of discrete analog (voltage or temperature) & digital inputs.
- Convert the analog inputs to digital values.
- Format the sampled data into Space Packets.
- Output the sampled formatted data either through CAN or PacketWire IF.
- Receive commands through CAN IF (only when in RTU mode).

Consists of

- Analog Front Mux
- Signal Conditioning Unit
- Sensor Biasing unit
- ADC
- Digital Input Sampler (Differential Inputs)
- Voltage Reference
- Memory
- Space Packet Generation unit
- PacketWire IF
- CAN IF
- Control and Test unit



Product Highlights

- 12-bit monotonic digitally autozeroed ADC.
- Up to 32 differential analog inputs (4, 8, 16 or 32 selectable) - (4 groups) independently configurable for voltage or temperature measurements.
- Both PRTs & NTCs temperature sensors supported.
- 16 differential digital inputs.
- Synchronous/Asynchronous (event driven) sampling.
- Various sampling frequencies supported (20 mHz - 4 KHz).

Key Characteristics

- 0.25μm IHP SiGe Fabrication Technology.
- Single power supply 3.3V (internal voltage regulator).
- Low power consumption ($<$20 mW).
- Wide Temperature Operating range (-75 to 145 deg C).
- Radhard up to 1 Mrad.
- Immune to SELs at 67 MeV/mg/cm^2.
- No SEFIs up to 67 MeV/mg/cm^2.
- SEU LET threshold between 32 and 40 MeV/mg/cm^2.

2 Applications

- Essential telemetry support in S/C.
- Remote Terminal Unit in space data acquisition systems.
- Housekeeping in space instrumentation.

3 Operation Characteristics

3.1 Analog and Digital Channels Sampling

The ETM samples all the Digital and Analog input Channels according to a predefined/fixed sequence, as shown in Fig. 1. The Digital Channels are sampled simultaneously at the beginning of the scan sequence, while the Analog ones sequentially and in a fixed/predefined order within a scan sequence. The time between sampling any two adjacent Analog Channels is equal and evenly distributed over the full scan sequence period. All channels are sampled with the same frequency.

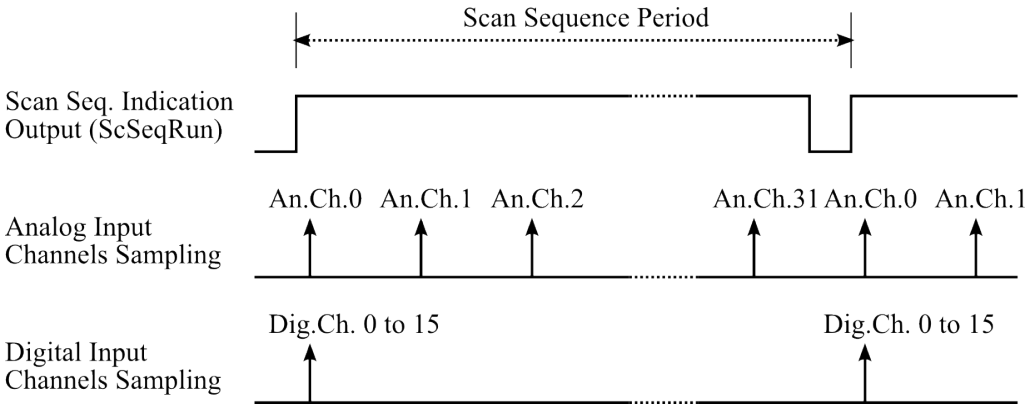


Figure 1: ETM Digital and Analog Channels Scanning/Sampling Sequence.

3.2 Number of Active Channels Sampled

The 32 Analog Channels are split into four signals groups (Sg0, Sg1, Sg2 and Sg3). Sg0 and Sg1 both contain 4 Analog Channels, while Sg2 and Sg3 contain 8 and 16 Analog Channels, respectively. The selection of the active groups is accomplished by means of two dedicated input pins (S_Sg[1..0]) as shown in Table 1. The Digital Channels are always sampled.

Table 1: ETM ASIC Analog Channels Signals Groups selection.

S_Sg[1..0]	An. Ch. Group Active	Comments
00	Sg0	only the first 4 An. Ch. are active
01	Sg0 & Sg1	only the first 8 An. Ch. are active
10	Sg0 & Sg1 & Sg2	only the first 16 An. Ch. are active
11	Sg0 & Sg1 & Sg2 & Sg3	all the 32 An. Ch. are active

3.3 Configuration of a Sampling Group

Each signal group can be independently configured for:

- Voltage measurements (ASMN mode).
- Temperature measurements (TSM mode) with passive sensors (PRTs, NTCs).
- Digital signal measurements (Digital mode). In this configuration the 12 bit successive approximation ADC is configured for 1 bit measurements.

The configuration for groups Sg0 and Sg1 together, Sg2 and Sg3 are independently selectable by means of six dedicated input pins (2 pins for Sg0 & Sg1 - S_Conf_Sg01[1..0], 2 pins for Sg2 - S_Conf_Sg2[1..0] and 2 pins for Sg3 - S_Conf_Sg3[1..0]), as shown in Table 2.

Table 2: ETM ASIC Analog Channels Signals Groups measurements configuration.

Sg Conf. Sel. Pins	ASMN	TSM	Digital
S_Conf_Sg01[1..0]	00	01	11
S_Conf_Sg2[1..0]	00	01	11
S_Conf_Sg3[1..0]	00	01	11

3.4 Differential and Single Ended Voltage Measurements

The ETM device can be used for both differential and single ended voltage measurements. Differential measurements are performed through sequential sampling of the positive and negative inputs of the channels and then by subtracting the ADC results. In order for the user to perform single ended measurements, the negative input of the analog channel needs to be grounded externally.

3.5 Temperature Measurements

ETM can be used for measuring temperatures from PRTs or NTCs by sourcing a user defined temperature and power supply independent current on the passive device and then quantizing the developed voltage by the 12 bit ADC. The block diagram of the temperature measurement unit is shown in Fig. 2. Assuming an ideal opamp, the current source output current is defined as

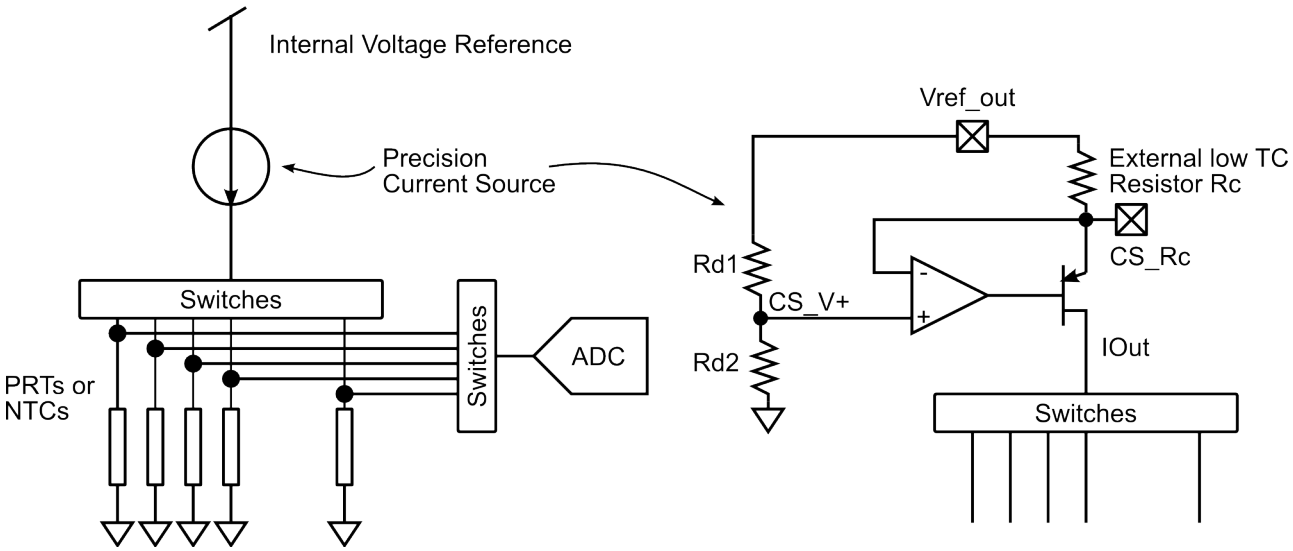


Figure 2: Block diagram of the ETM temperature measurement unit.

$$I_{OUT} = \frac{V_{ref\_out} \cdot (1 - \frac{R_{d2}}{R_{d1}+R_{d2}})}{R_C} \quad (1)$$

The voltage developed on the temperature sensor (R_{Sensor}) will be equal to

$$V_{Sensor} = \frac{V_{ref\_out} \cdot (1 - \frac{R_{d2}}{R_{d1}+R_{d2}})}{R_C} \cdot R_{Sensor} \quad (2)$$

Assuming a PRT temperature sensor, equation 2 becomes

$$V_{Sensor} = \frac{V_{ref\_out} \cdot (1 - \frac{R_{d2}}{R_{d1}+R_{d2}})}{R_C} \cdot R_{Sensor,0}(1 + TC_{Rs}\Delta\Theta) \quad (3)$$

where,
$R_{Sensor,0}$ is the resistance of the sensor at 0°C,
TC_{Rs} is the temperature coefficient of the sensor and
$\Delta\Theta$ is the temperature difference on the sensor from the reference temperature of 0°C.
The ADC quantization of the voltage developed on the sensor (reference voltage to the ADC is V_{ref_out}) will result in an output code equal to

$$OC = \frac{R_{Sensor,0}(1 + TC_{Rs}\Delta\Theta)}{R_C} \cdot (1 - \frac{R_{d2}}{R_{d1} + R_{d2}}) \quad (4)$$

From equation 4 the $\Delta\Theta$ parameter (sensor temperature) can be extracted. To achieve good temperature resolution it is advised that the external current setting resistor R_C has a temperature coefficient of 10 ppm/°C.
Important Note: Vref_Out is the voltage reference applied to the device. For more information look at section 3.6.

3.6 Reference Voltage for Voltage and Temperature Measurements

ETM contains a precision voltage reference that produces a temperature, power supply and TID independent voltage close to 1.2V. ETM can be configured in the following ways:

- Amplify the internal voltage reference and then apply it to the ADC.
- Apply an external voltage reference to the amplification unit and then apply it to the ADC.
- Apply an external voltage reference directly to the ADC.

3.6.1 Application of the Internal Voltage Reference to the ADC

The internal voltage reference is amplified before being applied to the ADC as shown in Fig. 3. The user can define the gain through external resistors R_{F1} and R_{F2}. The gain is defined as

$$X2_{GAIN} = (1 + \frac{R_{F1}}{R_{F2}}) \quad (5)$$

The maximum gain value that can be applied is limited by the fact that the output of the amplifier can not exceed 2.5V.

3.6.2 Application of an External Voltage Reference to the ETM ASIC

Alternatively, the user can disable the internal voltage reference and provide an external voltage to the input of the X2 amplifier as shown in Fig. 4. As it can be seen in this case to save power (1mW) the internal voltage reference can be disabled by setting pad *iBG_En* to GND.

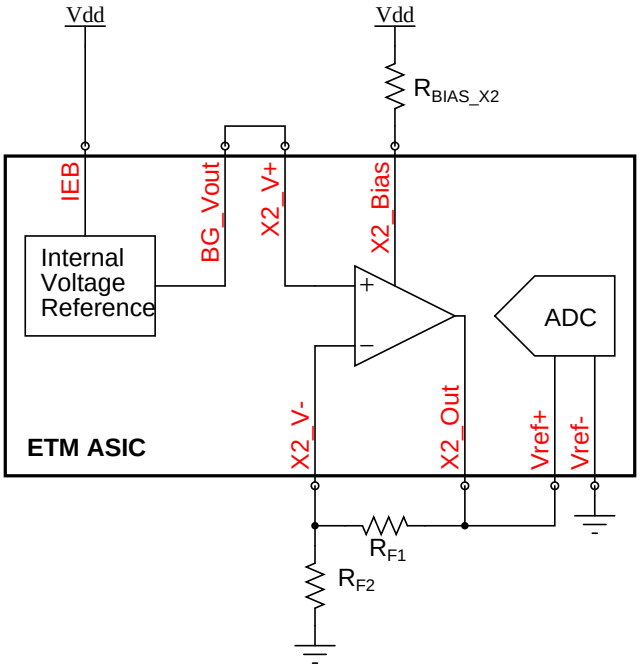


Figure 3: Schematic of the circuitry that is used to amplify the internal voltage reference to a suitable level for the ADC.

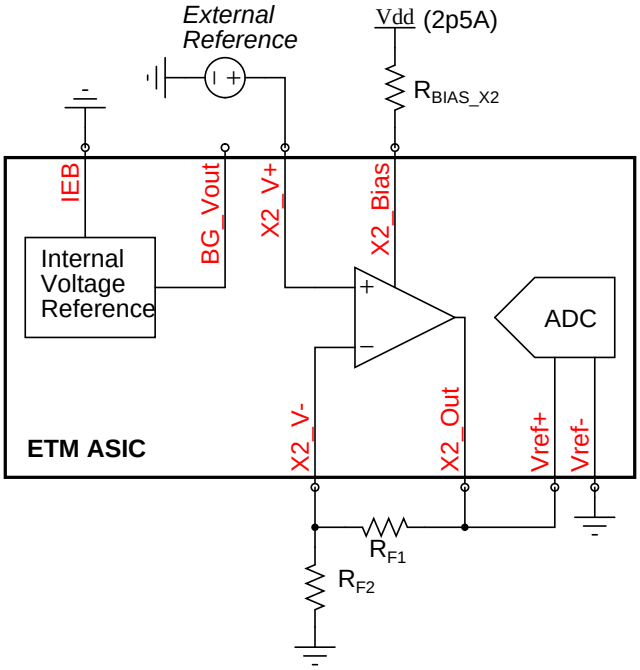


Figure 4: Application of an external voltage reference to the ETM ASIC without bypassing the X2 amplifier.

3.6.3 Application of a Voltage Reference Directly to the ADC

Furthermore, the user can apply a voltage reference directly to the ADC as shown in Fig. 5. In this case the bias of the X2 amplifier can be shut down by connecting node *X2_Bias* to GND saving another 1mW from the total power.

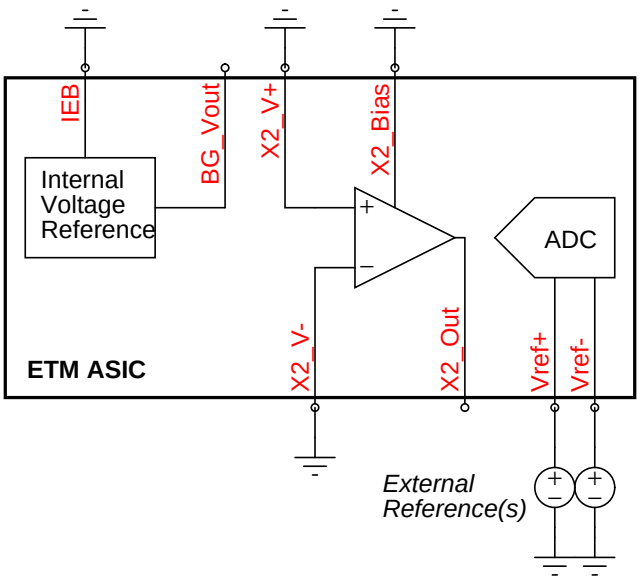


Figure 5: Application of an external voltage reference to the ETM ASIC bypassing the X2 amplifier.

3.7 Digital Sampling Functionality

ETM has the capability to sample 16 differential digital inputs. The sampling circuit is shown in Fig. 6. It consists of a comparator, a source follower to implement the threshold shift and an input multiplexer.

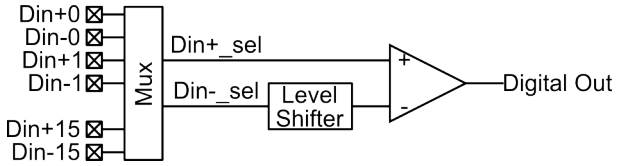


Figure 6: Block diagram of the Digital Sampler circuit.

Functionality

$$V_{OUT} = \begin{cases} 1 & , D_{IN+} - D_{IN-} > V_{THR} \\ 0 & D_{IN+} - D_{IN-} < V_{THR} \end{cases}$$

where D_{IN+} and D_{IN-} are the differential terminals and V_{THR} is a user defined threshold voltage.

The voltage shift of the source follower, which is also the threshold voltage of the Digital Sampler can be defined by the user through pad *pSF_bias*.

3.8 Sampling Frequency

The sampling frequency (the rate at which each input is scanned) can be selected between 20 mHz and 4 KHz (assuming a 16 MHz master clock), through hard pins (S_ScSeqPer[4..0], S_SysClk, S_Sg[1..0]). In RTU mode the value of the S_ScSeqPer[4..2] and S_SysClk parameters can also be set by a command through CAN bus, which has priority over the respective hard pins settings (see Fig. 14). This feature allows the user to change the sampling frequency on flight.

In Tables 3 and 4 all the supported sampling frequencies / scan sequence periods for ETM Master Clock (MClk) of 16 MHz, as well as all the Analog Channels to Channel sampling intervals, both in us or ms (for ETM MClk of 16 MHz) and in number of MClk pulses are listed.

Table 3: Input Channels Sampling Frequencies / Scan Sequence Periods
for **SysClk High 1.6 MHz (S_SysClk=1)** at **16 MHz Master Clock**.

S_ScSeqPer[4..0]	S_Sg[1..0]=00 (Sg0 active)	S_Sg[1..0]=01 (Sg0,1 active)	S_Sg[1..0]=10 (Sg0,1,2 active)	S_Sg[1..0]=11 (Sg0,1,2,3 active)	Samples Interval
00000	500Hz / 2ms	500Hz / 2ms	500Hz / 2ms	500Hz / 2ms	62.5us / 10^3MClk
00001	1KHz / 1ms	1KHz / 1ms	1KHz / 1ms	invalid	62.5us / 10^3MClk
00010	2KHz / 500us	2KHz / 500us	invalid	invalid	62.5us / 10^3MClk
00011	4KHz / 250us	invalid	invalid	invalid	62.5us / 10^3MClk
00100	200Hz / 5ms	200Hz / 5ms	200Hz / 5ms	200Hz / 5ms	156.25us / 2.5x10^3MClk
00101	400Hz / 2.5ms	400Hz / 2.5ms	400Hz / 2.5ms	invalid	156.25us / 2.5x10^3MClk
00110	800Hz / 1.25ms	800Hz / 1.25ms	invalid	invalid	156.25us / 2.5x10^3MClk
00111	1.6KHz / 625us	invalid	invalid	invalid	156.25us / 2.5x10^3MClk
01000	100Hz / 10ms	100Hz / 10ms	100Hz / 10ms	100Hz / 10ms	312.5us / 5x10^3MClk
01001	200Hz / 5ms	200Hz / 5ms	200Hz / 5ms	invalid	312.5us / 5x10^3MClk
01010	400Hz / 2.5ms	400Hz / 2.5ms	invalid	invalid	312.5us / 5x10^3MClk
01011	800Hz / 1.25ms	invalid	invalid	invalid	312.5us / 5x10^3MClk
01100	50Hz / 20ms	50Hz / 20ms	50Hz / 20ms	50Hz / 20ms	625us / 10^4MClk
01101	100Hz / 10ms	100Hz / 10ms	100Hz / 10ms	invalid	625us / 10^4MClk
01110	200Hz / 5ms	200Hz / 5ms	invalid	invalid	625us / 10^4MClk
01111	400Hz / 2.5ms	invalid	invalid	invalid	625us / 10^4MClk
10000	20Hz / 50ms	20Hz / 50ms	20Hz / 50ms	20Hz / 50ms	1.5625ms / 2.5x10^4MClk
10001	40Hz / 25ms	40Hz / 25ms	40Hz / 25ms	invalid	1.5625ms / 2.5x10^4MClk
10010	80Hz / 12.5ms	80Hz / 12.5ms	invalid	invalid	1.5625ms / 2.5x10^4MClk
10011	160Hz / 6.25ms	invalid	invalid	invalid	1.5625ms / 2.5x10^4MClk
10100	10Hz / 100ms	10Hz / 100ms	10Hz / 100ms	10Hz / 100ms	3.125ms / 5x10^4MClk
10101	20Hz / 50ms	20Hz / 50ms	20Hz / 50ms	invalid	3.125ms / 5x10^4MClk
10110	40Hz / 25ms	40Hz / 25ms	invalid	invalid	3.125ms / 5x10^4MClk
10111	80Hz / 12.5ms	invalid	invalid	invalid	3.125ms / 5x10^4MClk
11000	5Hz / 200ms	5Hz / 200ms	5Hz / 200ms	5Hz / 200ms	6.25ms / 10^5MClk
11001	10Hz / 100ms	10Hz / 100ms	10Hz / 100ms	invalid	6.25ms / 10^5MClk
11010	20Hz / 50ms	20Hz / 50ms	invalid	invalid	6.25ms / 10^5MClk
11010	40Hz / 25ms	invalid	invalid	invalid	6.25ms / 10^5MClk
11100	2Hz / 500ms	2Hz / 500ms	2Hz / 500ms	2Hz / 500ms	15.625ms / 2.5x10^5MClk
11101	4Hz / 250ms	4Hz / 250ms	4Hz / 250ms	invalid	15.625ms / 2.5x10^5MClk
11110	8Hz / 125ms	8Hz / 125ms	invalid	invalid	15.625ms / 2.5x10^5MClk
11111	16KHz / 62.5ms	invalid	invalid	invalid	15.625ms / 2.5x10^5MClk

Table 4: Input Channels Sampling Frequencies / Scan Sequence Periods
for **SysClk Low 16 KHz (S_SysClk=0)** at **16 MHz Master Clock**.

S_ScSeqPer[4..0]	Sg0 active	Sg0&1 active	Sg0&1&2 active	Sg0&1&2&3 active	Samples Interval
00000	5Hz / 200ms	5Hz / 200ms	5Hz / 200ms	5Hz / 200ms	6.25ms / 10^5MClk
00001	10Hz / 100ms	10Hz / 100ms	10Hz / 100ms	invalid	6.25ms / 10^5MClk
00010	20Hz / 50ms	2KHz / 50ms	invalid	invalid	6.25ms / 10^5MClk
00011	40Hz / 25ms	invalid	invalid	invalid	6.25ms / 10^5MClk
00100	2Hz / 500ms	2Hz / 500ms	2Hz / 500ms	2Hz / 500ms	15.625ms / 2.5x10^5MClk
00101	4Hz / 250ms	4Hz / 250ms	4Hz / 250ms	invalid	15.625ms / 2.5x10^5MClk
00110	8Hz / 125ms	8Hz / 125ms	invalid	invalid	15.625ms / 2.5x10^5MClk
00111	16KHz / 62.5ms	invalid	invalid	invalid	15.625ms / 2.5x10^5MClk
01000	1Hz / 1s	1Hz / 1s	1Hz / 1s	1Hz / 10ms	31.25ms / 5x10^5MClk
01001	2Hz / 500ms	2Hz / 500ms	2Hz / 500ms	invalid	31.25ms / 5x10^5MClk
01010	4Hz / 250ms	4Hz / 250ms	invalid	invalid	31.25ms / 5x10^5MClk
01011	8Hz / 125ms	invalid	invalid	invalid	31.25ms / 5x10^5MClk

Cont. –

– Cont.					
S_ScSeqPer[4..0]	**Sg0 active**	**Sg0&1 active**	**Sg0&1&2 active**	**Sg0&1&2&3 active**	**Samples Interval**
01100	0.5Hz / 2s	0.5Hz / 2s	0.5Hz / 2s	0.5Hz / 2s	62.5ms / 10^6MClk
01101	1Hz / 1s	1Hz / 1s	1Hz / 1s	invalid	62.5ms / 10^6MClk
01110	2Hz / 500ms	2Hz / 500mss	invalid	invalid	62.5ms / 10^6MClk
01111	4Hz / 250ms	invalid	invalid	invalid	62.5ms / 10^6MClk
10000	0.2Hz / 5s	0.2Hz / 5s	0.2Hz / 5s	0.2Hz / 5s	156.25ms / 2.5x10^6MClk
10001	0.4Hz / 2.5s	0.4Hz / 2.5s	0.4Hz / 2.5s	invalid	156.25ms / 2.5x10^6MClk
10010	0.8Hz / 1.25s	0.8Hz / 1.25s	invalid	invalid	156.25ms / 2.5x10^6MClk
10011	1.6 Hz / 0.625s	invalid	invalid	invalid	156.25ms / 2.5x10^6MClk
10100	0.1Hz / 10s	0.1Hz / 10s	0.1Hz / 10s	0.1Hz / 10s	312.5ms / 5x10^6MClk
10101	0.2Hz / 5s	0.2Hz / 5s	0.2Hz / 5s	invalid	312.5ms / 5x10^6MClk
10110	0.4Hz / 2.5s	0.4Hz / 2.5s	invalid	invalid	312.5ms / 5x10^6MClk
10111	0.8Hz / 1.25s	invalid	invalid	invalid	312.5ms / 5x10^6MClk
11000	0.05Hz / 20s	0.05Hz / 20s	0.05Hz / 20s	0.05Hz / 20s	625ms / 10^7MClk
11001	0.1Hz / 10s	0.1Hz / 10s	0.1Hz / 10s	invalid	625ms / 10^7MClk
11010	0.2Hz / 5s	0.2Hz / 5s	invalid	invalid	625ms / 10^7MClk
11010	0.4Hz / 2.5s	invalid	invalid	invalid	625ms / 10^7MClk
11100	0.02Hz / 50s	0.02Hz / 50s	0.02Hz / 50s	0.02Hz / 50s	1.5625s / 2.5x10^7MClk
11101	0.04Hz / 25s	0.04Hz / 25s	0.04Hz / 25s	invalid	1.5625s / 2.5x10^7MClk
11110	0.08Hz / 12.5s	0.08Hz / 12.5s	invalid	invalid	1.5625s / 2.5x10^7MClk
11111	0.16Hz / 6.25s	invalid	invalid	invalid	1.5625s / 2.5x10^7MClk

3.9 Scan Sequence Control

The ETM supports a control mechanism for enabling/disabling the scan sequence and consequently the sampling and data transmission functions. This capability, offered via both, a particular input pin configuration (ScSeqEn - see Table 5) and a CAN command, allows the user to temporarily or permanently set the ASIC in standby mode, in order to reserve power and bandwidth resources, or inhibit the operation of a faulty device.

Table 5: Scan Sequence Enable/Disable selection.

ScSeqEn	Scan Sequence Activation
0	Disabled
1	Enabled

3.10 Scan Sequence Indication

The ETM provides an output signal (ScSeqRun) indicating that the scan sequence is running. This signal is asserted at the beginning of each scan sequence and stays high until it is de-asserted, when the last active analog channel is being sampled, as shown in Fig. 7. The shape/waveform and timing of this signal is indicative of the boundaries (start and completion) of each scan sequence. The Analog Channel to Channel sampling intervals, in number of MClk pulses, when *SysClk* is high and when *SysClk* is low, are given in Tables 3 and 4, respectively.

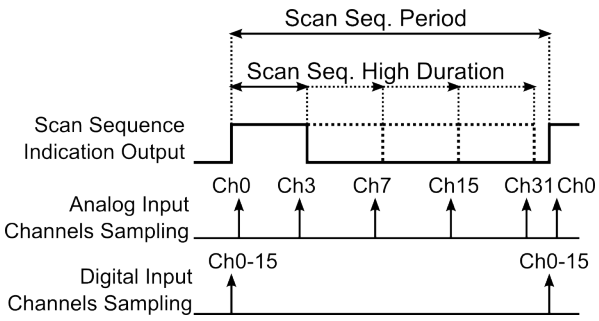


Figure 7: Timing characteristics of output ScSeqRun.

In tables 6 and 7 the duration (in Master Clock pulses) while output ScSeqRun is high and the period of this signal are shown.

Table 6: Scan sequence period/scan sequence high duration in Master Clock pulses for **S_SysClk** High.

S_ScSeqPer[4..0]	S_Sg[1..0]=00 (Sg0 active)	S_Sg[1..0]=01 (Sg0,1 active)	S_Sg[1..0]=10 (Sg0,1,2 active)	S_Sg[1..0]=11 (Sg0,1,2,3 active)
00000	$32x10^3/3.995x10^3$	$32x10^3/7.995x10^3$	$32x10^3/15.995x10^3$	$32x10^3/31.995x10^3$
00001	$16x10^3/3.995x10^3$	$16x10^3/7.995x10^3$	$16x10^3/15.995x10^3$	invalid
00010	$8x10^3/3.995x10^3$	$8x10^3/7.995x10^3$	invalid	invalid
00011	$4x10^3/3.995x10^3$	invalid	invalid	invalid
00100	$8x10^4/9.995x10^3$	$8x10^4/19.995x10^3$	$8x10^4/39.995x10^3$	$8x10^4/79.995x10^3$
00101	$4x10^4/9.995x10^3$	$4x10^4/19.995x10^3$	$4x10^4/39.995x10^3$	invalid
00110	$2x10^4/9.995x10^3$	$2x10^4/19.995x10^3$	invalid	invalid
00111	$1x10^4/9.995x10^3$	invalid	invalid	invalid
01000	$1.6x10^5/19.995x10^3$	$1.6x10^5/39.995x10^3$	$1.6x10^5/79.995x10^3$	$1.6x10^5/159.995x10^3$
01001	$8x10^4/19.995x10^3$	$8x10^4/39.995x10^3$	$8x10^4/79.995x10^3$	invalid
01010	$4x10^4/19.995x10^3$	$4x10^4/39.995x10^3$	invalid	invalid
01011	$2x10^4/19.995x10^3$	invalid	invalid	invalid
01100	$3.2x10^5/39.995x10^3$	$3.2x10^5/79.995x10^3$	$3.2x10^5/159.995x10^3$	$3.2x10^5/319.995x10^3$
01101	$1.6x10^5/39.995x10^3$	$1.6x10^5/79.995x10^3$	$1.6x10^5/159.995x10^3$	invalid
01110	$8x10^4/39.995x10^3$	$8x10^4/79.995x10^3$	invalid	invalid
01111	$4x10^4/39.995x10^3$	invalid	invalid	invalid
10000	$8x10^5/99.995x10^3$	$8x10^5/199.995x10^3$	$8x10^5/399.995x10^3$	$8x10^5/799.995x10^3$
10001	$4x10^5/99.995x10^3$	$4x10^5/199.995x10^3$	$4x10^5/399.995x10^3$	invalid
10010	$2x10^5/99.995x10^3$	$2x10^5/199.995x10^3$	invalid	invalid
10011	$1x10^5/99.995x10^3$	invalid	invalid	invalid
10100	$1.6x10^6/199.995x10^3$	$1.6x10^6/399.995x10^3$	$1.6x10^6/799.995x10^3$	$1.6x10^6/1599.995x10^3$
10101	$8x10^5/199.995x10^3$	$8x10^5/399.995x10^3$	$8x10^5/799.995x10^3$	invalid
10110	$4x10^5/199.995x10^3$	$4x10^5/399.995x10^3$	invalid	invalid
10111	$2x10^5/199.995x10^3$	invalid	invalid	invalid
11000	$3.2x10^6//399.995x10^3$	$3.2x10^6/799.995x10^3$	$3.2x10^6/1599.995x10^3$	$3.2x10^6/3199.995x10^3$
11001	$1.6x10^6/399.995x10^3$	$1.6x10^6/799.995x10^3$	$1.6x10^6/1599.995x10^3$	invalid
11010	$8x10^5/399.995x10^3$	$8x10^5/799.995x10^3$	invalid	invalid
11010	$4x10^5$ /$399.995x10^3$	invalid	invalid	invalid
11100	$8x10^6/999.995x10^3$	$8x10^6/1999.995x10^3$	$8x10^6/3999.995x10^3$	$8x10^6/7999.995x10^3$
11101	$4x10^6/999.995x10^3$	$4x10^6/1999.995x10^3$	$4x10^6/3999.995x10^3$	invalid
11110	$2x10^6/999.995x10^3$	$2x10^6/1999.995x10^3$	invalid	invalid
11111	$1x10^6/999.995x10^3$	invalid	invalid	invalid

Table 7: Scan sequence period/scan sequence high duration in Master Clock pulses for **S_SysClk** Low.

S_ScSeqPer[4..0]	S_Sg[1..0]=00 (Sg0 active)	S_Sg[1..0]=01 (Sg0,1 active)	S_Sg[1..0]=10 (Sg0,1,2 active)	S_Sg[1..0]=11 (Sg0,1,2,3 active)
00000	$32x10^5/3.995x10^5$	$32x10^5/7.995x10^5$	$32x10^5/15.995x10^5$	$32x10^5/31.995x10^5$
00001	$16x10^5/3.995x10^5$	$16x10^5/7.995x10^5$	$16x10^5/15.995x10^5$	invalid
00010	$8x10^5/3.995x10^5$	$8x10^5/7.995x10^5$	invalid	invalid
00011	$4x10^5/3.995x10^5$	invalid	invalid	invalid
00100	$8x10^6/9.995x10^5$	$8x10^6/19.995x10^5$	$8x10^6/39.995x10^5$	$8x10^6/79.995x10^5$
00101	$4x10^6/9.995x10^5$	$4x10^6/19.995x10^5$	$4x10^6/39.995x10^5$	invalid
00110	$2x10^6/9.995x10^5$	$2x10^6/19.995x10^5$	invalid	invalid
00111	$1x10^6/9.995x10^5$	invalid	invalid	invalid
01000	$1.6x10^7/19.995x10^5$	$1.6x10^7/39.995x10^5$	$1.6x10^7/79.995x10^5$	$1.6x10^7/159.995x10^5$
01001	$8x10^6/19.995x10^5$	$8x10^6/39.995x10^5$	$8x10^6/79.995x10^5$	invalid
01010	$4x10^6/19.995x10^5$	$4x10^6/39.995x10^5$	invalid	invalid
01011	$2x10^6/19.995x10^5$	invalid	invalid	invalid
01100	$3.2x10^7/39.995x10^5$	$3.2x10^7/79.995x10^5$	$3.2x10^7/159.995x10^5$	$3.2x10^7/319.995x10^5$
01101	$1.6x10^7/39.995x10^5$	$1.6x10^7/79.995x10^5$	$1.6x10^7/159.995x10^5$	invalid
01110	$8x10^6/39.995x10^5$	$8x10^6/79.995x10^5$	invalid	invalid
01111	$4x10^6/39.995x10^5$	invalid	invalid	invalid
10000	$8x10^7/99.995x10^5$	$8x10^7/199.995x10^5$	$8x10^7/399.995x10^5$	8x107/799.995x10^5

Cont. –

– Cont.				
S_ScSeqPer[4..0]	**Sg0 active**	**Sg0&1 active**	**Sg0&1&2 active**	**Sg0&1&2&3 active**
10001	$4x10^7/99.995x10^5$	$4x10^7/199.995x10^5$	$4x10^7/399.995x10^5$	invalid
10010	$2x10^7/99.995x10^5$	$2x10^7/199.995x10^5$	invalid	invalid
10011	$1x10^7/99.995x10^5$	invalid	invalid	invalid
10100	$1.6x10^8/199.995x10^5$	$1.6x10^8/399.995x10^5$	$1.6x10^8/799.995x10^5$	$1.6x10^8/1599.995x10^5$
10101	$8x10^7/199.995x10^5$	$8x10^7/399.995x10^5$	$8x10^7/799.995x10^5$	invalid
10110	$4x10^7/199.995x10^5$	$4x10^7/399.995x10^5$	invalid	invalid
10111	$2x10^7/199.995x10^5$	invalid	invalid	invalid
11000	$3.2x10^8//399.995x10^5$	$3.2x10^8/799.995x10^5$	$3.2x10^8/1599.995x10^5$	$3.2x10^8/3199.995x10^5$
11001	$1.6x10^8/399.995x10^5$	$1.6x10^8/799.995x10^5$	$1.6x10^8/1599.995x10^5$	invalid
11010	$8x10^7/399.995x10^5$	$8x10^7/799.995x10^5$	invalid	invalid
11010	$4x10^7$ /399.995x10^5	invalid	invalid	invalid
11100	$8x10^8/999.995x10^5$	$8x10^8/1999.995x10^5$	$8x10^8/3999.995x10^5$	$8x10^8/7999.995x10^5$
11101	$4x10^8/999.995x10^5$	$4x10^8/1999.995x10^5$	$4x10^8/3999.995x10^5$	invalid
11110	$2x10^8/999.995x10^5$	$2x10^8/1999.995x10^5$	invalid	invalid
11111	$1x10^8/999.995x10^5$	invalid	invalid	invalid

4 Sampled Data Packet Generation

4.1 Space Packet Format

The ETM, independently from the selected operating mode (STD, CSC/DC or RTU), organizes the sampled data into Space Packet (SP) format, according to [D1], section 4. The generated SPs consist of two major fields, the Packet Primary Header and the Packet Data, positioned contiguously as shown in table 8.

Table 8: ETM Space Packet Format

Field	**Packet Primary Header**	**Packet Data**			
		Sampled Data Dig. & An. Ch. Data	**Time of Origin Stamp**	**Anomaly Indication**	**Error Control**
Mandatory / Optional	Optional	Mandatory	Optional	Optional	Optional
Size (octets)	6	3-50	0 to 4	0 or 1	0 or 2

The Packet Primary Header field identifies the source and the characteristics of the Space Packet. It consists of four sub-fields (Packet Version Number, Packet Identification, Packet Sequence Control and Packet Data Length) positioned contiguously, as shown in table 9.

Table 9: Space Packet Primary Header Format.

Packet Version Number	**Packet Identification**			**Packet Sequence Control**		**Packet Data Length**
	Packet Type	**Secondary Header Flag**	**Application Process ID**	**Sequence Flags**	**Packet Sequence Count**	
Bits 0-2	Bit 3	Bit 4	Bits 5-15	Bits 16-17	Bits 18-31	Bits 32-47
000 fixed	**0 fixed**	**0 fixed**	**Configurable by the user**	**11 fixed**	**Internally provided**	**Variable**

The Packet Data field consists of four sub-fields (Sampled Data, Time of Origin Stamp, Anomaly Indication and Error Control) positioned contiguously, as shown in table 8.

- The Sampled Data sub-field, starts with the Digital Channels data which is followed by the Analog Channels data. The 1st bit of the Digital Channels data corresponds to Digital Channel 15. The first Analog Channels data corresponds to Analog Channel 0 (starting with the MSb of the 12-bit value). The size of this sub-field is not fixed but varies depending on the number of active Analog Channels (S_Sg[1..0]), and the ADC mode (12-bit or 1-bit conversion) for each active channels group (S_Conf_Sg01[1..0], S_Conf_Sg2[1..0] and S_Conf_Sg3[1..0]).
- The Time of Origin Stamp (TOS) sub-field includes time information that allows the determination of the absolute start time of the scan sequence and consequently of the sampling time of each channel. The size and kind of the included information depend on the combination of: (1) the Operating Mode configuration pin setting (S_ETM_Conf), (2) the configured (by a Processor Module command) ETM's operation parameters/settings (synchronous/asynchronous and CANopen SYNC messages availability) and (3) the TOS selection pins settings (S_TOS[2..0]).
- The Anomaly Indication sub-field includes the status of anomaly flags that indicate specific irregular conditions, traced during the previous scan sequence period, concerning: the successful transportation of the generated SPs inside the scan sequence period boundaries and the error conditions met during the communication over the CAN Bus. The inclusion or not of this sub-field in the SPs is selectable by means of a dedicated input pin (S_Pack_AnIndic).
- The Error Control sub-field includes a 16-bit CRC (defined in [D5]) error detection code which allows the detection of errors that have been introduced into the SP by the lower layers (during the transmission process or during other processing or storage activities), and therefore it can be used to verify that the integrity of the complete SP has been preserved. The inclusion or not of this sub-field is selectable by means of a dedicated input pin (S_Pack_ErrCntr).

The ETM can be configured to generate SPs without Packet Primary Header field (simplified SPs). The selection among generating standard or simplified SPs is accomplished by means of a dedicated input pin (S_Pack_Std_SimplN), as shown in Table 10.

Table 10: ETM ASIC Standard/Simplified Space Packet generation selection.

S_Pack_Std_SimplN	ETM ASIC Generated SP
0	Simplified (without Packet Primary Header field)
1	Standard (with Packet Primary Header field)

Each particular ETM, independently from its operating mode, is identified by a unique 11-bit Application Process Identifier (APID), set through eleven dedicated input pins (APID[10..0]). This APID number allows distinguishing the ETM from which telemetry data (SPs) originate (see Fig. 9) as well as addressing the ETM(s) in RTU mode.
Restriction: Some specific values of the APID (0 and 2040 to 2047 decimal - see [D1]) are reserved by CCSDS for special uses and cannot be used for the ETM applications.

4.2 ETM Space Packet Size

The ETM is capable of generating SPs with different length depending on the settings of the following configuration input pins:

- the S_Pack_Std_SimplN that defines the inclusion or not of the Packet Primary Header field
- the S_Sg[1..0] that define the active Analog Channels groups (Sg0, Sg1, Sg2, Sg3)
- the S_Conf_Sg01[1..0], S_Conf_Sg2[1..0] and S_Conf_Sg3[1..0] that define the Analog Channels groups configuration for analogue (ASMN, TSMN1 & 2) or digital signals (1-bit sample) sampling

- the S_TOS[2..0] that define the size of the TOS sub-field
- the S_Pack_AnIndic that defines the inclusion or not of the Anomaly Indication sub-field
- the S_Pack_ErrCntr that defines the inclusion or not of the Error Control sub-field

However, a particular ETM generates SPs with fixed length, provided that all the above settings are fixed during its operation.
The number of bits of the Space Packet is calculated according to equation 6.

$$SP_{Size} = SPacket_{Std\_Simpl} \cdot 48 + 16 + ADC_{Bits} + TOS_{Param} \cdot 8 + An_{Indic} \cdot 8 + Error_{Control} \cdot 16 \quad (6)$$

The TOS$_{Param}$ values depending on $TOS[2..0]$ settings are listed in equation 7.

$$TOS_{Param} = \begin{cases} 0 & \text{if } TOS[2..0] = 000, \\ 1 & \text{if } TOS[2..0] = 001, \\ 2 & \text{if } TOS[2..0] = 010, \\ 3 & \text{if } TOS[2..0] = 100, \\ 3 & \text{if } TOS[2..0] = 101, \\ 4 & \text{if } TOS[2..0] = 111. \end{cases} \quad (7)$$

The ADC_{Bits} parameter (needed in equation 6) is calculated according to equations 8 through 11.

$$ADC_{Bits} = \begin{cases} ADC_{Bits,ChG01}/2 & \text{if } S\_SG[1..0] = 00, \\ ADC_{Bits,ChG01} & \text{if } S\_SG[1..0] = 01, \\ ADC_{Bits,ChG01} + ADC_{Bits,ChG2} & \text{if } S\_SG[1..0] = 10, \\ ADC_{Bits,ChG01} + ADC_{Bits,ChG2} + ADC_{Bits,ChG3} & \text{if } S\_SG[1..0] = 11. \end{cases} \quad (8)$$

$$ADC_{Bits,ChG01} = \begin{cases} 96 & \text{if } S\_Conf\_SG01[1..0] = 00, \\ 96 & \text{if } S\_Conf\_SG01[1..0] = 01, \\ 16 & \text{if } S\_Conf\_SG01[1..0] = 11 \text{ and } S\_SG[1..0] = 00, \\ 8 & \text{if } S\_Conf\_SG01[1..0] = 11 \text{ and } S\_SG[1..0] = 01. \end{cases} \quad (9)$$

$$ADC_{Bits,ChG2} = \begin{cases} 96 & \text{if } S\_Conf\_SG2[1..0] = 00, \\ 96 & \text{if } S\_Conf\_SG2[1..0] = 01, \\ 8 & \text{if } S\_Conf\_SG2[1..0] = 11. \end{cases} \quad (10)$$

$$ADC_{Bits,ChG3} = \begin{cases} 192 & \text{if } S\_Conf\_SG3[1..0] = 00, \\ 192 & \text{if } S\_Conf\_SG3[1..0] = 01, \\ 16 & \text{if } S\_Conf\_SG3[1..0] = 11. \end{cases} \quad (11)$$

Fig. 8 presents a graphical way of calculating the length of all possible SPs.

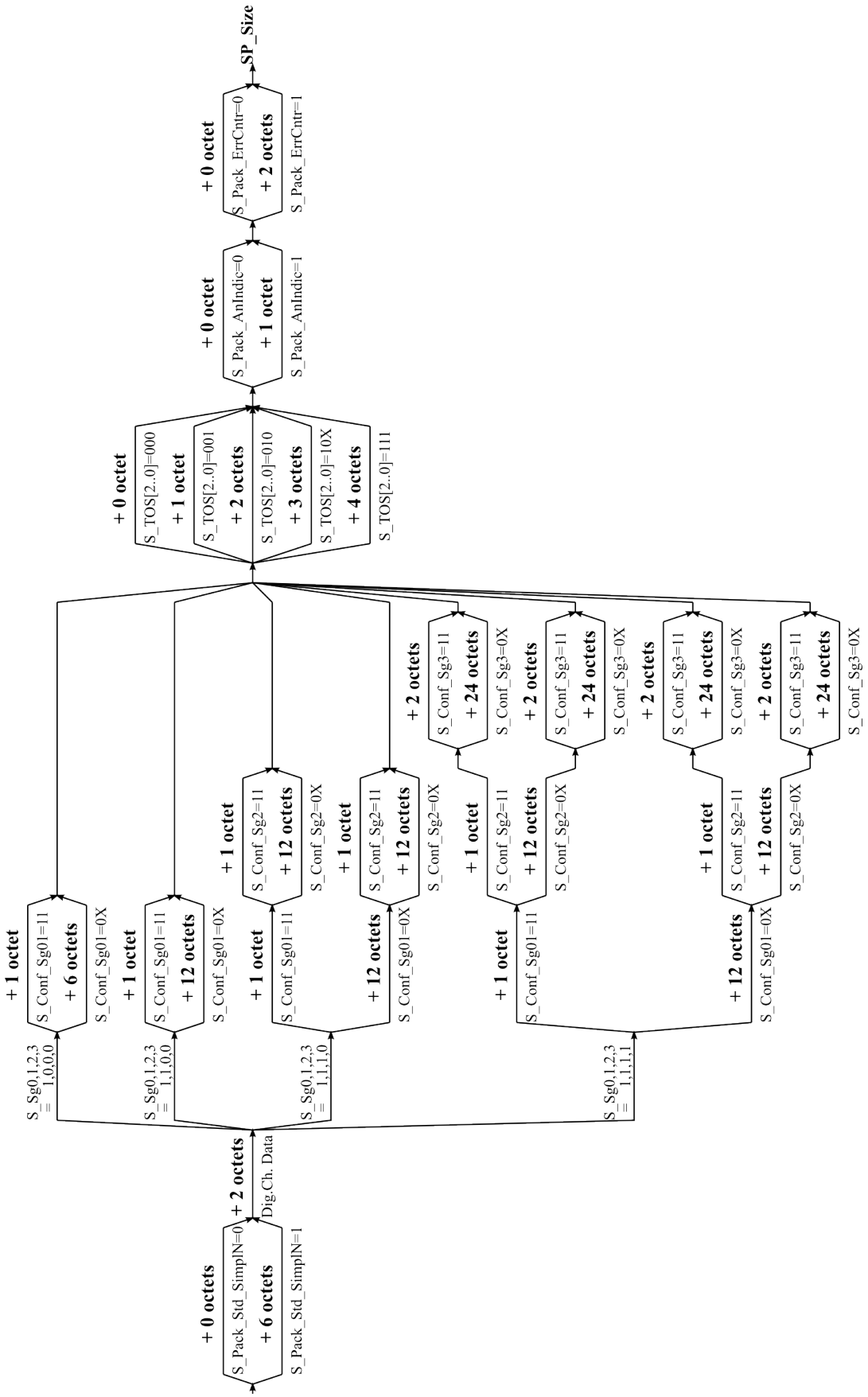


Figure 8: Space Packet Length Calculation.

4.3 ETM Space Packet Releasing

The ETM can be configured to operate in two different modes with respect to the SPs releasing (generation/transmission) method used. Its operation in one of these two modes is selected by means of a dedicated pin (S_Event_NormalN) as shown in Table 11.

Table 11: Selection of the ETM ASIC SPs releasing mode.

S_Event_NormalN	SPs Releasing Mode
0	Normal Mode
1	Event Mode

In Normal mode sampled data is acquired in each scan sequence period and is transmitted at the beginning of the next scan sequence period.

In Event mode sampled data is acquired in each scan sequence period and is transmitted at the beginning of the next scan sequence period only in the following cases:

- when any of the discrete Digital Channels inputs has changed compared with its previously sampled value
- periodically every 65536 sampling sequences, even in case that no event occurs within this time period

This allows the generation of packets only in case of a specific event, while ensures that a packet will be generated periodically even in case that no event occurs within this time period.

4.4 Space Packet Fields

4.4.1 TOS Field

The purpose of the Time of Origin Stamp (TOS) field is to allow the determination of the absolute start time of the scan sequence and consequently of the absolute sampling time of each channel. ETM uses an absolute time reference signal (Time Strobe pulse) and the relative offset of the next scan sequence start time to calculate the absolute start time of the scan sequence.
To allow unambiguous datation the ETM counts the number of:

- External Time Strobe pulses received since Power-on or Master reset, and of
- ETM System Clocks that have elapsed between the assertion of the Time Strobe signal and the start of the next of the relevant scan sequence period,

and incorporate these information into the TOS field of each generated Space Packet, as shown in Table 12. A Time Strobe pulse (positive edge triggered pulse with duration greater than 1 MClk - that is greater that 62.5ns in case of a 16MHz MClk), whenever asserted, triggers the internal 8-bit *Time Strobe Counter* (which counts the received Time Strobe pulses). Especially in STD and CSC/DC ETM configurations the Time Strobe pulse, whenever asserted, simultaneously resets the internal 24-bit *Free Running Counter*, which in this cases counts the number of ETM System Clocks that have elapsed between the assertion of the Time Strobe pulse and the start of the next of the relevant scan sequence period.
In case of Non-synchronized RTU ETM configuration, and if no SYNC messages are broadcasted over the CAN Bus, the ETM uses its internal *Scan Sequence Increment* signal, instead of its System Clock, to trigger the 24-bit *Free Running Counter*. The Overflow of this 24-bit counter, in turn, triggers the 8-bit *Time Strobe Counter* (see also above). Instead, in cases of Synchronized or Non-synchronized RTU ETM configurations, with SYNC messages periodically broadcasted over the CAN

Bus, a ”Sync” pulse, generated by its CAN I/F whenever a SYNC message received, is used to trigger the 24-bit *Free Running Counter*. Again, the Overflow of this 24-bit counter triggers the 8-bit *Time Strobe Counter*.
The format of the TOS field is shown in Fig. 9.

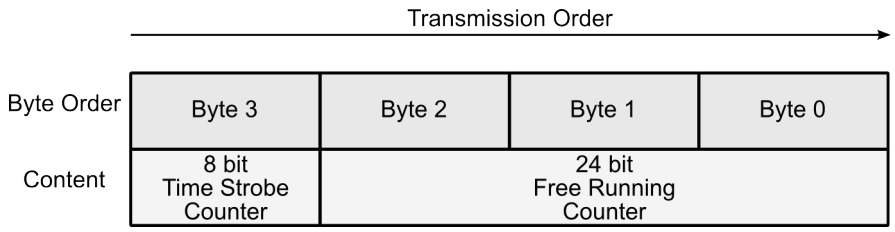


Figure 9: TOS field transmission order. In this case it is assumed that all TOS fields are transmitted.

The available TOS configurations are presented in Table 12.

Table 12: Time of Origin Stamp (TOS - Datation) field alternatives.

S_TOS[2..0]	Length (Bytes)	Timing Information included into Space Packet
000	0	A TOS field is not included into the Space Packet
001	1	The content of the 8-bit Time Strobe Counter
010	2	Only the 16 LSbs of the 24-bit Free Running Counter
100	3	The entire content of the 24-bit Free Running Counter
101	3	The 16 LSbs of the 24-bit Free Running Counter plus the content of the 8-bit Time Strobe Counter
111	4	The entire content of the 24-bit Free Running Counter plus the content of the 8-bit Time Strobe Counter

4.4.2 Anomaly Indication Field

The Anomaly Indication field contains information regarding the real time operational characteristics of the ETM device. The format of the Anomaly Indication field is shown in Fig. 10.

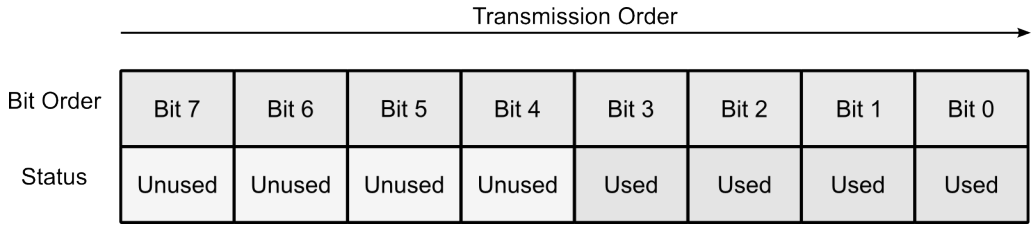


Figure 10: Information on the used flag bits of the Anomaly Indication Field.

Bit 0,1 (Buffer Overwrite flags 1 and 2): Both flags indicate that the data of at least one scan sequence (that is one or more Space Packets (SP)) have been lost (never sent) due to unavailability of the PW link (in STD and CSC/DC modes) or due to increased traffic on the CAN bus (in RTU mode). Specifically,

- flag1 indicates that the transmission of the previous SP, in comparison to the one that holds the flag, was extended in more than one Scan Sequence period, and thus the memory buffer that holds the sampled data of the currently transmitted SP has been overwritten at least one time
- flag 2 indicates that the previously sampled data (that is one SP), in comparison to the data of the Space Packet that holds the flag, has been lost (never sent) because the previous SP transmission could not start during the time frame of the previous scan sequence period.

It is noted that lost SP(s) transmission is not detectable though monitoring the ”Packet Sequence Count” field of the SPs, which reflects only the number of successfully transmitted SPs. The only way to notice missing SP(s) transmission, apart from these two anomaly indication flags, is through analysis of the SP timing information (TOS field), if its inclusion in the SP is activated.

Bit 2 (CAN Error Threshold flag): If high it indicates that at least one of the two CAN Controller Error Counters has exceeded the value 96. This, recommended by the Bosch standard, indication suggests that either the CAN bus is heavily disturbed or the ETM device on the bus is producing errors.This flag is valid only in RTU mode.

Bit 3 (CAN Error Passive flag): If high it indicates that at least one of the two CAN Controller Error Counters has exceeded the value 128 and the specific ETM's CAN interface has entered in error-passive mode. This flag is valid only in RTU mode.

It should be noted that, for the Anomaly Indication field to be included in the space packet, the pin S_Pack_Indic needs to be high.

5 Communication Interfaces

Two different serial interfaces, the PacketWire (PW) and the CAN, are implemented into the ETM ASIC to cover its communication needs (data transfers, control/configuration and monitoring).

5.1 PacketWire Interface

The ETM's PW IF is a serial synchronous output IF, compliant with the SCTMTC TM Encoder VCs' PW Input IF, defined in [D2].
It is responsible for the ETM SPs transmission to the SCTMTC TM encoder in STD and CSC/DC operating modes, while is kept reset in RTU mode. Its connection on the PW link is established through four signals shown in Table 13.

Table 13: ETM PW IF I/Os.

	IOs	Functionality
PW_TmeSRdy	I	Indicates the SCTMTC availability to receive data (High)
PW_TmeSValid	O (tri-state)	Indicates to the SCTMTC that Valid Data are put on the link (High)
PW_TmeSOut	O (tri-state)	Serial data line where data are shifted on, one bit at a time, at the falling edge of the PW_TmeSClk
PW_TmeSClk	O (tri-state)	Clock by which the SCTMTC samples (rising edge) the PW_TmeSOut serial data

In STD mode the tri-state output drivers are permanently active. In CSC/DC mode only the tri-state drivers of the ETM that has access to the link at that time are active.

A representative shot of the PW IF I/Os timing during SPs transmission is shown in Fig. 28. The timing characteristics of these signals are presented in Table 30.

5.1.1 Selecting Transmission Rates of the PW Interface

The PW output IF data rate is selectable, as shown in table 14, through control pins S_PW/CAN_BR[1..0]).

Table 14: ETM PW IF Baud Rate Configuration, with respect to Master Clock Frequency (F_MClk), Selection.

S_PW/CAN_BR[1..0]	PW IF Baud Rate Supported
00	F_MClk
01	F_MClk/2
10	F_MClk/4
11	F_MClk/16

5.2 CAN Bus Interface

The ETM's CAN IF is a 1 Mbps, non-redundant CAN Bus IF, compliant with the mandatory and some of the optional requirements specified in [D3].
It allows the communication, through CAN Bus, between ETM and the Processor Module (PM) in case of RTU mode configuration, while it is kept reset in STD and CSC/DC modes. Specifically, the RTU ETM (CAN slave) sends to the PM (CAN master), through its CAN IF, the sampled channels and status/confirmation data and receive from the PM configuration/control commands and synchronization.
The CAN IF consists of :

- A CAN Controller, which implements the lowest Data Link and part of the Physical layers of the CAN protocol version 2.0 B ([D4]).
- A simplified CANopen module, implementing, in compliance with [D3], the mandatory services of the CANopen protocol (an Application layer of the CAN protocol), that is required for ETM to manage its communication (for control/commanding, monitoring, data transfers and synchronization) via CAN Bus.
- A Large Data Unit Transfer (LDUT) protocol implementation (compliant with [D3]), with configurable transmission type (synchronous or asynchronous/on-event) and COB-ID, which coexists / collaborates with the CANopen protocol and used for sending the ETM large data units (SPs), encapsulated in successive CAN frames, over the CAN Bus to the PM.

Apart from the 1 Mbps, the 500 Kbps, 250 Kbps and 125 Kbps baud rates are also supported by the ETM CAN IF implementation. The selected baud rate is set by two dedicated pins (S_CAN_BR[1..0]) as shown in Table 15.
The CAN IF implementation allows the direct connection to a board external CAN bus via a CAN transceiver compliant with [D3], section 5. This is accomplished through the CAN_TXD output and CAN_RXD input pins of the ASIC.

5.2.1 CANopen Functionality

The CANopen module performs the following functions:

Table 15: ETM CAN IF Baud Rate Configuration Selection.

S_PW/CAN_BR[1..0]	CAN IF Baud Rate Supported
00	1 Mbps
01	500 Kbps
10	250 Kbps
11	125 Kbps

- Sends a Boot-up message with a predefined COB-ID after Reset
- Recognizes Network Management (NMT) messages with a predefined COB-ID
- Recognizes SYNC messages with a programmable COB-ID
- Sends periodic Heartbeat messages with a predefined COB-ID
- Supports one Client and one Server Service Data Object (SDO) with predefined COB-IDs that are used to:
    1. configure the following:
        - ETM System clock frequency (High/Low)
        - ETM Sampling frequency (Scan Sequence Period)
        - ETM SP releasing mode (Normal/Event)
        - ETM operation in synchronous (LDUT transmission type: 1, 2 or up to 240 SYNC messages) or Asynchronous - On Event mode (LDUT transmission type: 254)
        - The availability or not of SYNC messages on the CAN Bus for extracting time stamp information when the ETM is configured in non-synchronized RTU operation mode
        - Specific fields of the COB-ID of the supported CANopen communication object which is assigned to LDUT protocol
        - The Heartbeat messages transmission periodicity (from 1 ms up to 65.5 sec)
        - The COB-ID of the SYNC message
    2. confirm the above configuration process and notify, when requested, the ETM's configuration/settings to CAN master.

All the communication objects supported by the ETM's CANopen implementation use COB-IDs of 11 bits (standard CAN). These COB-IDs, apart from the one used by the SYNC object, which is configurable, are predefined/fixed. Respectively, the LDUT protocol implementation uses a COB-ID of 29-bit (extended CAN), which can be configured through a SDO Download message by the CAN master.

5.2.2 CANopen Operation

Upon power-up the CANopen module sends a Boot-up message to the CAN master (PM), indicating its Node-ID and that the node is in service, and enters into Pre-Operational state. At this state, where the module will not transmit any LDUT messages, it enters in a loop waiting to be configured and activated by the master. While in Pre-Operational state the CANopen module is able to receive NMT and SDO messages and transmit SDO confirmations (only expedited SDO download transactions are supported). After having being configured, the CANopen enter the Operational state by means of an NMT message. At this state full communication capabilities are active. The CANopen can receive NMT messages, receive and transmit SDOs, transmit Heartbeat messages and LDUT packets. The exact operation of the LDUT module (transmitter) will depend on the selected LDUT transmission type.In the case of asynchronous transmission type (Non-synchronized RTU configuration), the

module will forward the collected data to the CAN Controller as soon as this are available (at the beginning of each scan sequence period). On the contrary, in the case of synchronous transmission type (Synchronized RTU configuration), a number of SYNC messages shall be received before data transmission. The number of SYNC messages before the transmission of a LDUT packet will be defined during configuration at the Pre-Operational state.
Space Packets will be transmitted as sequences of CAN frames that form LDUT packets. The module supports the following LDUT Frame Types at the transmit direction:

- Un-segmented data: for the case where an entire Space Packet fits a single CAN frame
- Data First Segment: the frame type for the first CAN frame of a LDUT packet
- Data Continuation Segment: the frame type for all CAN frames of a LDUT packet, except for the first and the last ones
- Data Last Segment: the frame type for the last CAN frame of a LDUT packet

Except for data transmission, upon the reception of a SYNC message the module triggers the start of a new scan sequence period (new sampling cycle).
The format of all the messages that the ETM CANopen supports (transmit/receive) is presented in Fig. 11, Fig. 12 and Fig. 13.

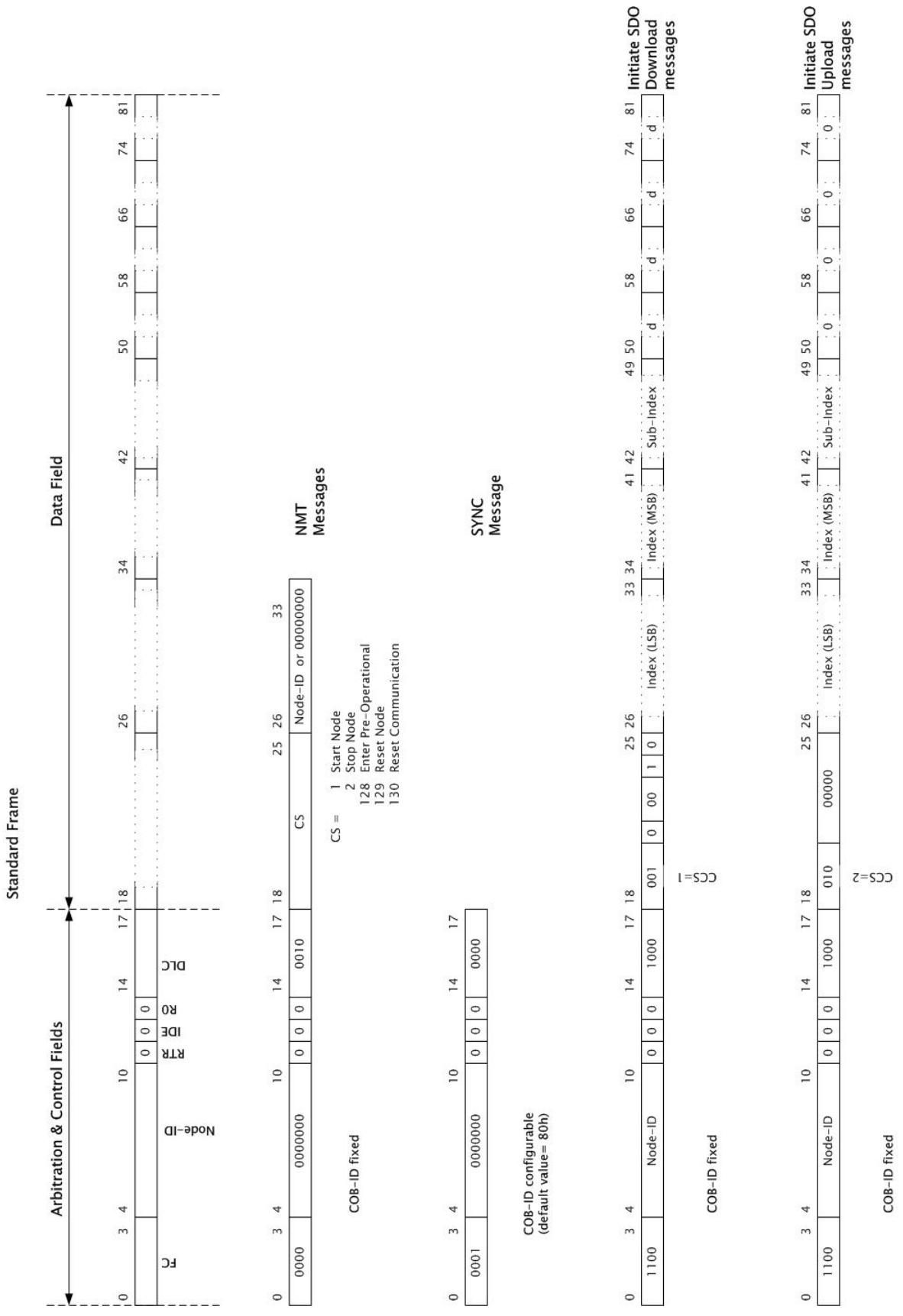


Figure 11: Format of the ETM CANopen Module received messages (CAN standard).

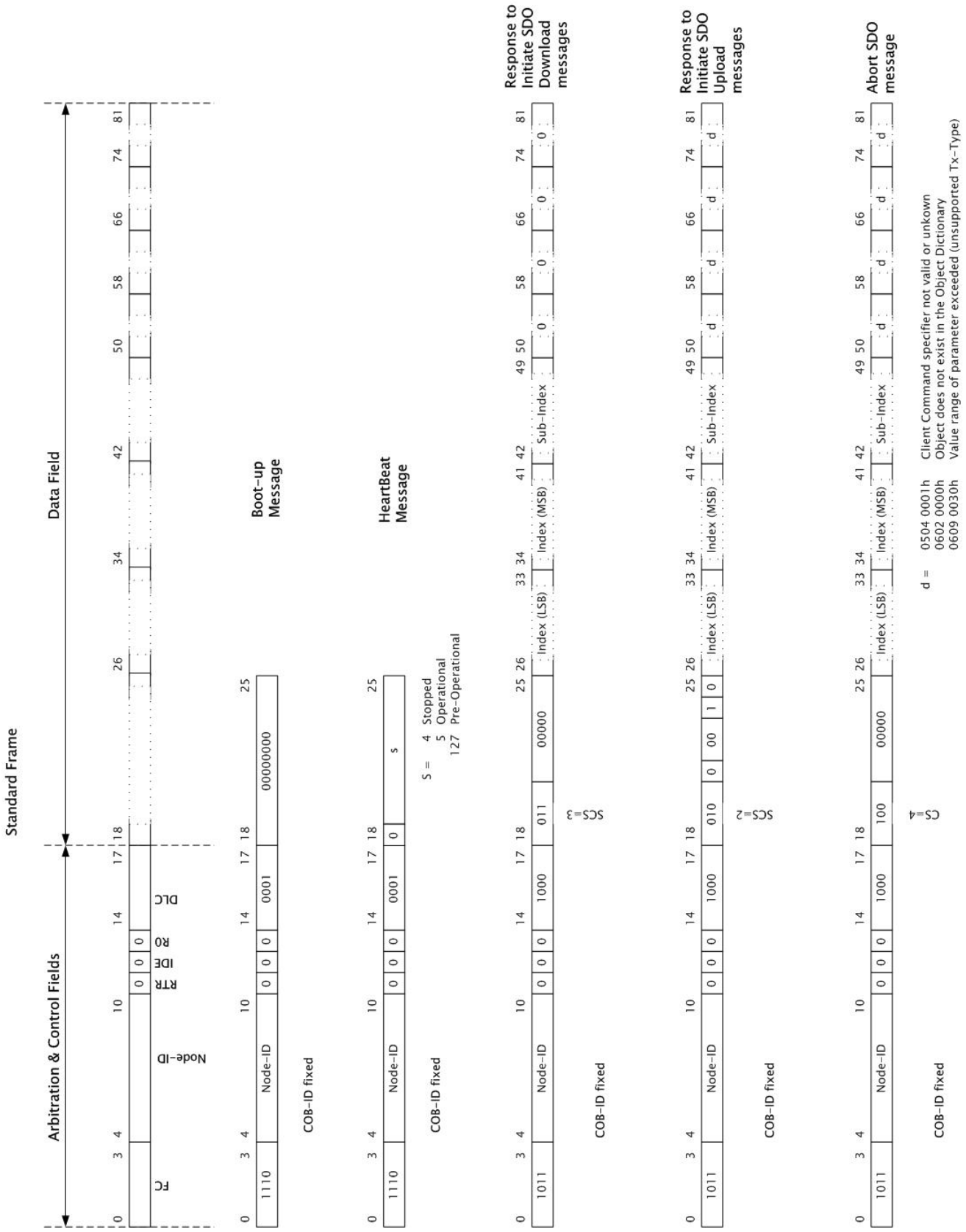


Figure 12: Format of the ETM CANopen Module transmitted messages (CAN standard).

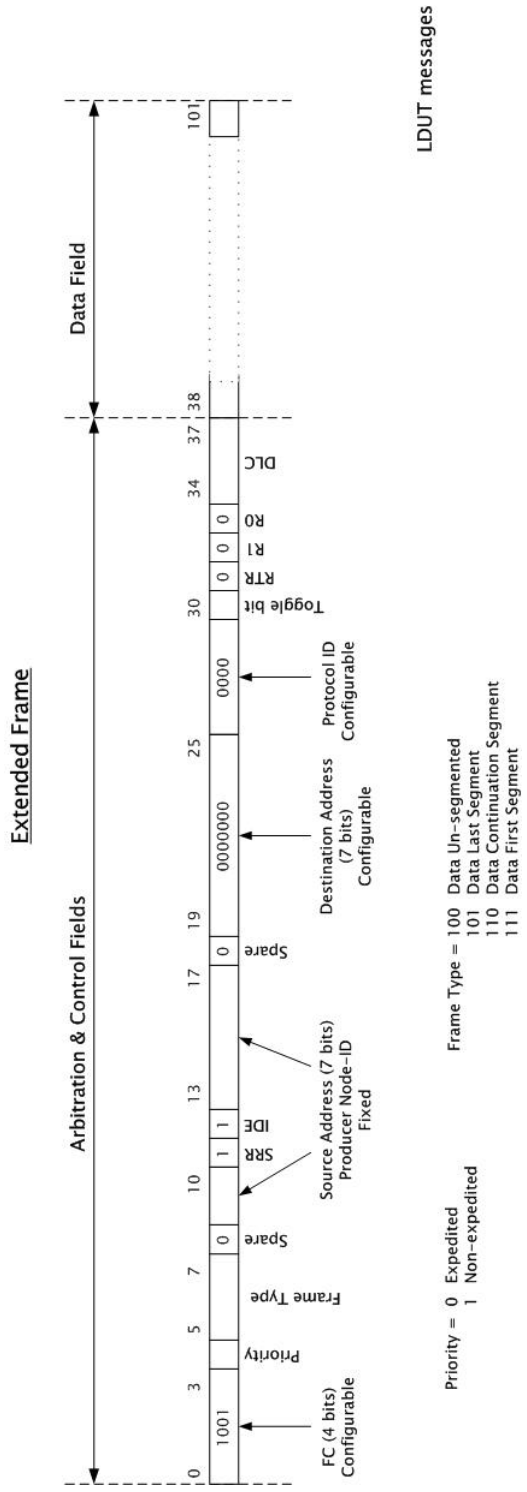


Figure 13: Format of the ETM CANopen Module LDUT transmitted messages (CAN extended).

The ETM operation in RTU mode is determined by a limited set of entries (objects) stored in the CANopen's Object Dictionary (OD) that are listed in Table 16.

Table 16: ETM CANopen OD entries.

Name	Index	Sub-Index	Type	Description
SYNC COB-ID Register	1005h	00h	Unsigned 16 (11 LSbs are used only)	Defines the COB-ID used for the recognition of a SYNC message
Heartbeat Register	1017h	00h	Unsigned 16	Defines the Heartbeat message periodicity in ms
ETM Control Register	2000h	00h	Unsigned 32 (8 LSbs are used only)	Controls parameters of the ETM operation such as the sampling frequency, the System Clock frequency etc.
ETM Status Register	2000h	00h	Unsigned 32 (8 LSbs are used only)	Reflects parameters of the ETM operation such as the sampling frequency, the System Clock frequency etc
LDUT No. of Entries	2100h	00h	Unsigned 8 (Read only object with a value of 0x2)	Number of supported LDUT Object sub-entries
LDUT COB-ID Register	2100h	01h	Unsigned 32	COB-ID used by the LDUT messages (for the ETM Space Packets transmission)
LDUT Tx-Type Register	2100h	02h	Unsigned 8	Defines the LDUT packets transmission scheme used (Non synchronized - Synchronized at the defined no. of received SYNC messages)

The format of the ETM Control Register is shown in Fig. 14.

- The SYNC Messages Availability field defines if SYNC messages are available on the CAN Bus (by the CAN master) for extracting time stamp information (applicable only when the ETM is configured in Non-synchronized RTU mode). Upon power-up this bit is reset (0 - no SYNC messages availability).
- The Sampling Frequency field defines the input channels Sampling Frequency. Upon power-up its value is determined by the level of the respective three pins S_ScSeqPer[4..2].
- The System Clock field determines the frequency of the selected ETM System clock. Upon power-up its value is determined by the level of the respective pin S_SysClk.
- The ETM Mode defines the SPs releasing mode (Normal or Event). Upon power-up its value is determined by the level of the respective pin S_Event_NormalN.

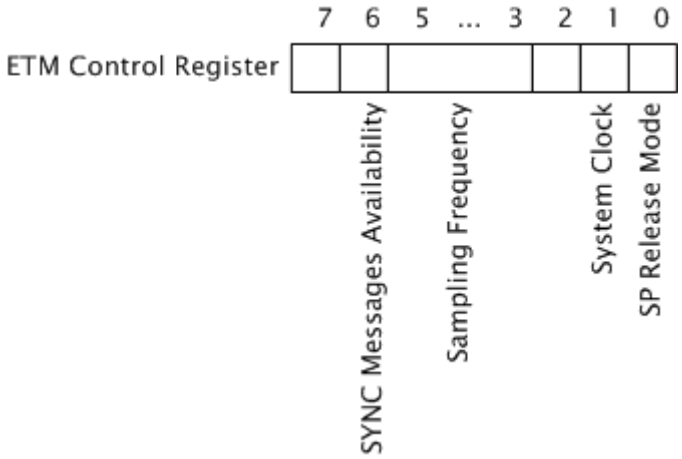


Figure 14: Format of the ETM Control Register.

The format of the ETM Status Register is identical to that of the Control Register. The Control register is a write only register. The Status Register is a read-only register.
It is noted that any change of the Control Register content (by means of a SDO download message), while the ETM is in Operational state, affects/reconfigures its operation at the beginning of the next scan sequence (at the ScSeqRun rising edge).

5.2.3 SDO Download Initiation Message Parameters

ETM responds only to expedited SDO download initiation messages. This means that, as shown in Fig. 11, the download requests must have **the first data byte set to 0x22hex**. The following table shows the separate SDO fields with details about the values of the first data byte within a SDO download initiation message.

Table 17: SDO download initiation message format.

Field	ccs	reserved	n	e	s	index	sub-index	data
Length	3 bits	1 bit	2 bits	1 bit	1 bit	2 bytes	1 byte	4 bytes
Expected ETM values	001	0	**00**	**1**	**0**	x	x	x

The meaning of each field is as follows:

- **ccs** is the client command specifier of the SDO transfer. It is 0 for SDO segment download, 1 for initiating download, 2 for initiating upload and 3 for SDO segment upload
- **n** is the number of bytes in the data part of the message which do not contain data, and it is only valid if e and s fields are set
- **e**, if set, indicates an expedited transfer, i.e. all data exchanged are contained within the message. If this bit is cleared then the message is a segmented transfer where the data does not fit into one message and multiple messages are used.
- **s**, if set, indicates that the data set size is specified in n field

ETM considers a received SDO download message as valid (responding with an SDO download confirmation message) only if its n (2 bits) and s fields (1 bit) are set to '0', and its e field (1 bit) is set to '1'. Otherwise it responds with an Abort SDO message with the "CCS not valid or unknown" abort code (0x05040001hex) in its data field.

6 Clocking Scheme

6.1 STD - CSC/DC Modes

There are two ways to clock the ETM ASIC in STD and CSC/DC modes:

- with an externally provided Master Clock on pad *MClk* with nominal frequency of 16 MHz or
- with a Master Clock signal generated by the ETM's internal clock oscillator.

The selection is performed by means of a dedicated pin (*S_MClk_Int_ExtN*) as shown in Table 18.

Table 18: ETM ASIC Master Clock (MClk) selection.

S_MClk_Int_ExtN	ETM ASIC MClk
0	External
1	Internal

6.2 Controlling the Output Frequency of the Internal Clock Oscillator

The output frequency of the internal clock oscillator can be controlled through pad *C_CLK*. In Fig.15 the typical output frequency versus the voltage on pad *C_CLK* is shown.

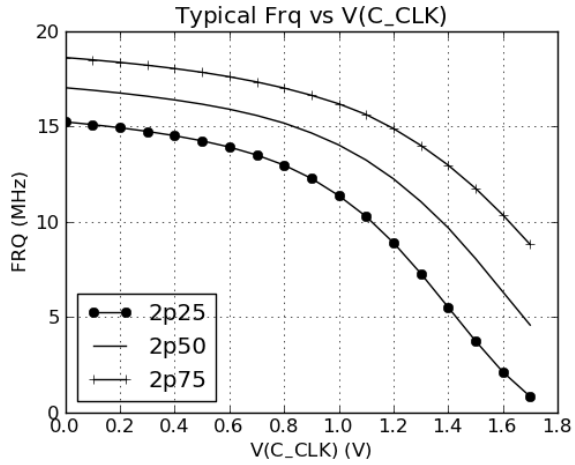


Figure 15: Clock oscillator frequency versus voltage on node *C_CLK* for all power supplies.

Notes on the performance and utilization of the internal oscillator:

- Temperature variation ranges from ±15% to ±5% depending on the output frequency.
- TID induced variation is less than 0.5% for doses up to 1MRad.
- It is advised that the user controls the voltage through an external resistive divider. To minimize jitter a capacitor can be also connected.

The internal clock oscillator is attarctive in some STD and CSC/DC ETM applications (where accurate TOS data and uniform sampling are not required), but an external oscillator is needed for RTU configuration, as the CAN specifications on oscillator characteristics are not covered by the internal ETM oscillator.

6.3 RTU Mode

In RTU mode there are two clock configurations:

- The entire ETM device operates on a single clock provided at pad *MClk*. In this case the clock has to meet the CAN standard specifications.

- The CAN interface operates on a clock provided at pad *CANIF_Clk* while the rest of the ASIC operates on a clock that is:
  - either provided externally on pad *MClk*
  - or produced internally through the on-chip oscillator,

  as described in section 6.1.

The selection is performed by means of a dedicated pad *TmStr/S_CANIF_Clk_In_ExtN* as shown in table 19.

Table 19: RTU Clock Configuration.

TmStr/S_CANIF_Clk_In_ExtN	ETM ASIC CAN IF Clock
0	Mclk
1	Clock provided at pad *CANIF_CLK*

6.3.1 Minimum and Maximum Clock Frequency in RTU Configuration

The minimum and maximum clock frequencies for the two configurations described above are listed in table 20.

Table 20: Minimum and maximum clock frequencies for the two RTU clock configurations.

Configuration	MClk (MHz)	CANIF_Clk (MHz)
Common Clock	16±1.58%	N/A
Two Clocks	8 - 24	16±1.58%

6.4 System Clock Selection

The ETM System Clock is the frequency used internally the ASIC for controlling the input channels sampling and the ADC. This signal is generated dividing the Master Clock by 10 (High SysClk) or 1000 (Low SysClk) depending on the ETM specific application needs. The selection of the preferred System Clock frequency is accomplished by means of a dedicated pin (S_SysClk) as shown in Table 21.

Table 21: ETM ASIC System Clock (SysClk) selection.

S_SysClk	ETM ASIC System Clock (SysClk)
0	16 KHz (Low SysClk)
1	1.6 MHz (High SysClk)

Alternatively, in RTU mode the hard pin selection can be overriden in flight through a command sent from the Processor Module via CAN Bus. In this case ETM's internal logic guaranties that the ongoing scan sequence is completed before the new selected System Clock frequency affects the ETM operation and its next scan sequences.

7 Initialization

The ETM supports four different ways for resetting the entire or part of the internal logic:

- Power-On-Reset-(POR)
- Master Reset
- NMT (Network Management) Node Reset
- NMT Communication Reset

The characteristics of these initialization mechanisms (the way of their assertion/de-assertion as well as the actions required for the ETM to start its nominal operation) are presented in Table 22.

Table 22: ETM ASIC Initialization mechanisms.

		STD & CSC/DC Modes	**RTU Mode**
Power-On-Reset: (POR pin)	**assertion**	entire logic on power-up	entire logic on power-up
	de-assertion	synchronously with MClk	synchronously with MClk
	oper. start	no action required	CANopen NMT Start command required
Master Reset: (MrExtN pin)	**assertion**	entire logic asynchronously	entire logic asynchronously
	de-assertion	synchronously with MClk	synchronously with MClk
	oper. start	no action required	CANopen NMT Start command required
NMT Node Reset: (Command through CAN Bus)	**assertion**	not applicable	entire logic synchr. through CANopen cmd.
	de-assertion	not applicable	synchronously with MClk
	oper. start	not applicable	CANopen NMT Start command required
NMT Com. Reset: (Command through CAN Bus)	**assertion**	not applicable	CAN IF only synchr. through CANopen cmd.
	de-assertion	not applicable	synchronously with MClk
	oper. start	not applicable	CANopen NMT Start command required

7.1 Power On Reset

When the power is switched on, the entire ETM logic is initialized (Power On Reset - POR), by means of an internal circuit, for 20 μsec. In case longer initialization time is required in a specific application, an external capacitor (e.g. a 40 nF capacitor will provide a 50 ms POR duration) has to be added from pad POR to GND as shown in Fig. 16.

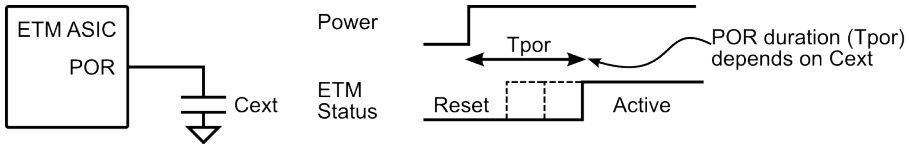


Figure 16: External capacitance to define the POR duration.

7.1.1 Confirmation of the POR Function Completion

The user can confirm that POR function has finished by the following means:

- **[STD and CSC/DC modes] -** By monitoring the *ScSq_Run* pad. After the POR function is finished, periodical pulses of programmable (configurable through specific pads) duration will be appeared on this pad, **provided that the *ScSq_En* pad is set high**.

- **[RTU mode] -** By getting a CANopen Boot-up message on the CAN bus.

7.2 Master Reset

The minimum Master Reset pulse (Low) duration required is one Master Clock (MClk) period.

7.3 Device During Power-off Mode

In case the device is powered off and a signal (analog voltage/digital input, digital setting or clock) is applied to its inputs the device will be turned on through the back to back protection diodes at the pads. If this situation persists for extended period of time (days) the device might get damaged. To protect the device against such a scenario, it is advised that all analog voltage and digital measurement inputs and all digital signals that can be high when the device is powered off are connected through 10 KΩ resistors as shown in Fig. 17.

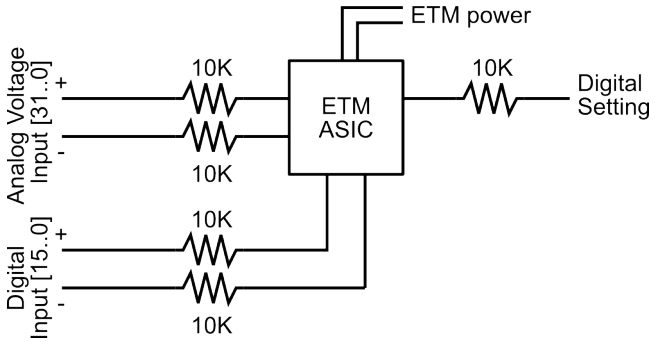


Figure 17: Connection of series resistors in the analog voltage and digital input channels so as not to power the device through these signals when it is powered off.

8 Operating Modes

The ETM ASIC can be configured to operate in the following three different modes, with respect to the communication interface used and its interconnection (if any) with other ETMs:

- Stand alone (STD)
- Cascaded/Daisy-Chain (CSC/DC)
- Remote Terminal Unit (RTU)

Its operating mode is selected by means of a dedicated pin (S_ETM_Conf) as shown in Table 23.

Table 23: ETM ASIC Operating Mode selection.

S_ETM_Conf	ETM ASIC Operating Mode
0	STD & CSC/DC
1	RTU

8.1 Stand Alone (STD) Operating Mode

The ETM ASIC configured in STD operating mode automatically performs its overall functionality (samples and digitizes predefined telemetries, formats the acquired data into SPs and forwards the packets via its PW IF to the SCTMTC ASIC TM encoder) immediately after power-on, without the need of user intervention. In this configuration the inputs S_Slave_MasterN and PW_Bus_GrantIn shall be fixed Low and High, respectively. A representative application of an ETM operating in STD mode is depicted in Fig. 18.

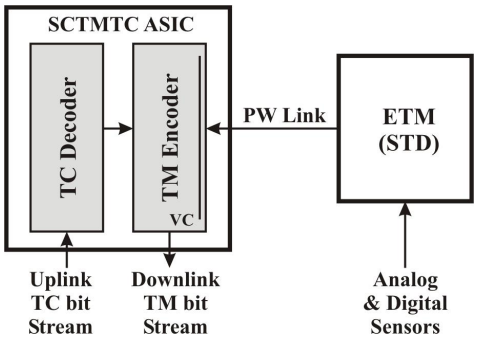


Figure 18: Application of an ETM operating in STD mode.

8.2 Cascaded/Daisy-Chain (CSC/DC) Operating Mode

The configuration of a number of ETM ASICs in CSC/DC operating mode, allows:

- the expansion of the number of the acquisition channels to be sampled,
- the devices connection, through a common PW link, to the same Virtual Channel (VC) input of the SCTMTC ASIC TM encoder.

One of the cascaded devices is configured as master (higher priority device), while the rest ones in the chain are configured as slaves (lower priority devices). The slaves priority, concerning the access to the PW link, is defined only by their relative position with respect to the master. The configuration of a device as master or slave is accomplished by means of a dedicated pin (S_Slave_MasterN) as shown in Table 24.

Table 24: CSC/DC ETM Master/Slave Configuration

S_Slave_MasterN	CSC/DC ETM Configuration
0	Master
1	Slave

All the cascaded devices start their operation simultaneously after power-on using common Master Clock (16 MHz). Their scan sequences are synchronized provided that they also have:

- the same settings, concerning the selected System Clock frequency and Scan Sequence Period,
- common Master Reset (MrExtN) and Scan Sequence Enable (ScSeqEn) inputs in order to be reset and/or enabled/disabled simultaneously.

At power-on the PW link is assigned to the master ETM. Each ETM in the chain transfers, in a priority order, the sampled data directly to the SCTMTC TM encoder, through its PW IF. The assignment of the PW link from one device to the next one in the chain is accomplished by means of two dedicated

pins, the PW_Bus_GrantOut and PW_Bus_GrantIn; the PW_Bus_GrantOut of each ETM is connected to the PW_Bus_GrantIn of the next one in the chain.
A representative application of three ETMs operating in CSC/DC mode is depicted in Fig. 19.

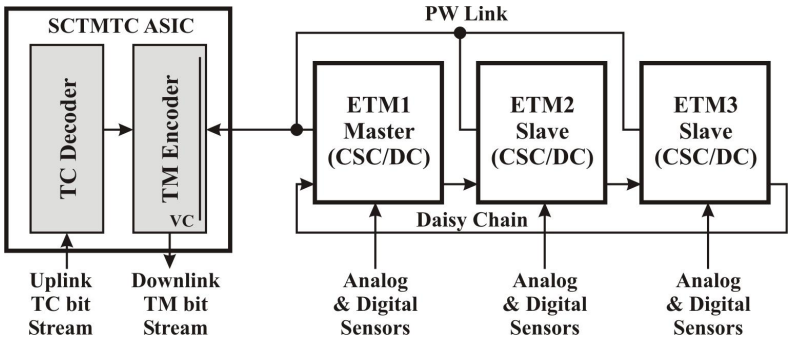


Figure 19: Application of three ETMs operating in CSC/DC mode.

8.3 Remote Terminal Unit (RTU) Operating Mode

In the case of their configuration in RTU operating mode the ETM ASICs (CAN Bus slaves) operating independently (synchronized or non-synchronized) sample and digitize predefined telemetries, organize the acquired data into SPs and forward the packets to the Processor Module (CAN Bus master) via CAN bus. The Processor Module (PM), apart from the sampled data reception, is responsible to control and synchronize (according to the specific application requirements) the ETMs' operations.

In case of their Synchronized operation all RTU ETMs shall have the same settings concerning the selected System Clock frequency and Scan Sequence Period. Their scan sequences are simultaneously triggered by SYNC messages which are periodically broadcasted by the PM over CAN Bus. Each ETM competes with the others to access (according to its priority - APID) the CAN Bus, in order to send the collected data. The data transmission periodicity (e.g. every 1, 2, or up to 240 SYNC messages) is programmable and may be different for each ETM on the CAN Bus.
It should be remarked here that the selected, by the system designer, SYNC messages broadcasting periodicity shall be greater than the selected ETMs scan sequence period. Otherwise the ETMs internal sampling logic will malfunction.

In case of their Non-synchronized (asynchronous - on event) operation all RTU ETMs may have different settings. Their scan sequences are triggered by their internal counters (on-event). Each ETM competes with the others to access the CAN Bus in order to send the collected data. This operation mode is further split into two sub-modes:

- In the first one SYNC messages are available (broadcasted by the PM) on the CAN Bus but they can be used by the Non-synchronized RTU ETMs only to derive time information.
- In the second one SYNC messages are not available at all and the Non-synchronized RTU ETMs have to use their internal clocks to derive time information.

The ETM supports its remote control/commanding directly from the PM via CAN Bus. The operation and communication parameters/settings which can be (re)programmed are:

- the System Clock Low/High frequency
- the Scan Sequence Period (S_ScSeqPer[4:2])
- the operation in Normal or Event mode
- the selected Synchronized/Non-synchronized operation
- the availability or not of SYNC messages for extracting time information when the ETM is configured in Non-synchronized (asynchronous) mode

- the data transmission periodicity every 1, 2 or up to 240 SYNC messages (applicable only in cases the synchronized ETM operation is selected)
- specific fields (e.g. COB-IDs) of the supported CAN protocol application layer's communication objects (e.g. of the LDUT protocol)

This SW (re)configuration of the ETMs operation has priority, overriding any already established HW (by means of dedicated pins) configuration. The ETM supports reading back by the PM, through the CAN Bus, all the above parameters/settings, in order to confirm their successful programming. A representative application of three ETMs operating in RTU mode is depicted in Fig. 20.

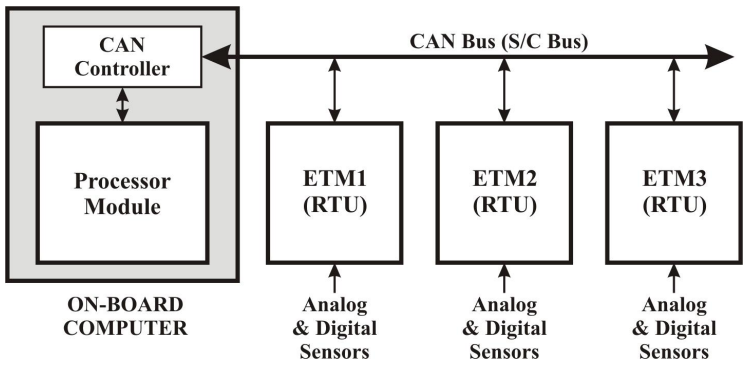


Figure 20: RTU ETMs configuration.

9 Electrical Characteristics

9.1 Maximum Ratings

The maximum ratings, which shall not be exceeded at any time during operation or storage, are listed in table 25.

Table 25: Maximum Ratings

Parameter	**Symbol**	**Max** & **Min Values**
Supply Voltage	Vdd	4V
Input Voltage Range	Vin	-1 to 6V
Input Current per power pin	I_{INP}	$\pm$50mA
Input/Output Current per signal pin	I_{INS}	$\pm$10mA
Operating Temperature Range	T_{OP}	-55 to +135 °C
Storage Temperature Range	T_{STG}	-65 to +150 °C
Soldering Lead Temp. 1.6 mm from case for max 10 s	T_{SOL}	+300 °C
Junction Temperature	T_J	+170 °C

9.2 Recommended Operating Conditions

The recommended operating conditions are listed in table 26.

Table 26: Recommended operating conditions.

Parameter	**Symbol**	**Max** & **Min Values**
Supply Voltage	VDD	3.0V dc to 3.6 V dc
Ambient Operating Temperature	T_A	-55 to 125 °C

10 Electrical Parameters

10.1 ADC

10.1.1 Missing Codes

There are no missing codes.

10.1.2 Monotonicity

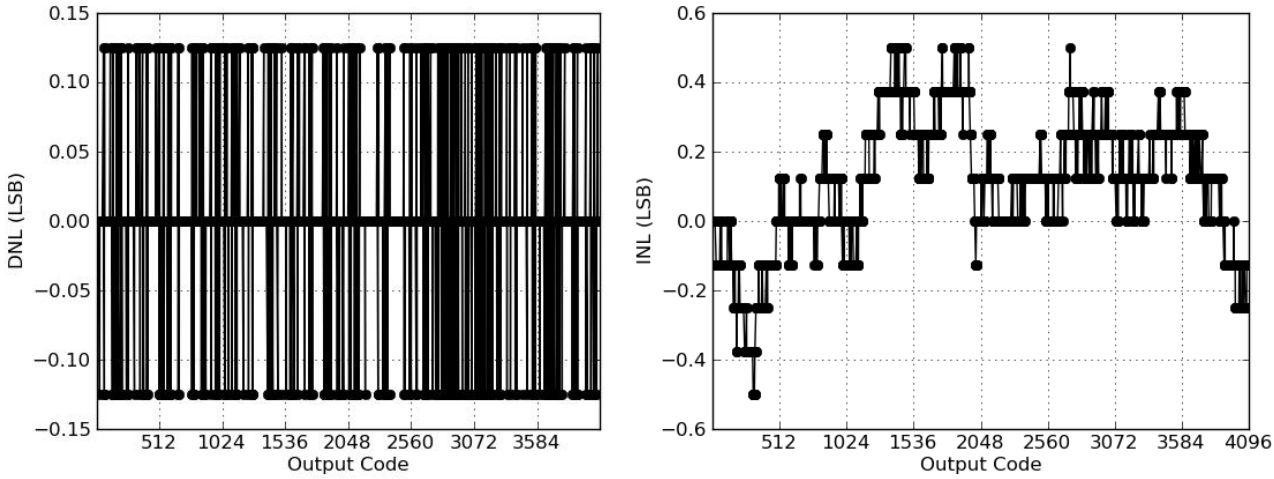
The ADC produces monotonic codes at all operating conditions.

10.1.3 DNL

A typical DNL curve is shown in Fig. 21.a.

10.1.4 INL

A typical INL curve is shown in Fig. 21.b.



(a) DNL (b) INL

Figure 21: Typical DNL and INL curves of the ETM device with Master Clock running at 16MHz.

10.2 The Voltage Reference

10.2.1 Internal Voltage Reference Performance

ETM contains a precision voltage reference. A typical output voltage versus temperature curve is shown in Fig. 22.
Power Supply Rejection is 84 dB at DC dropping to 80 dB at 100 KHz.

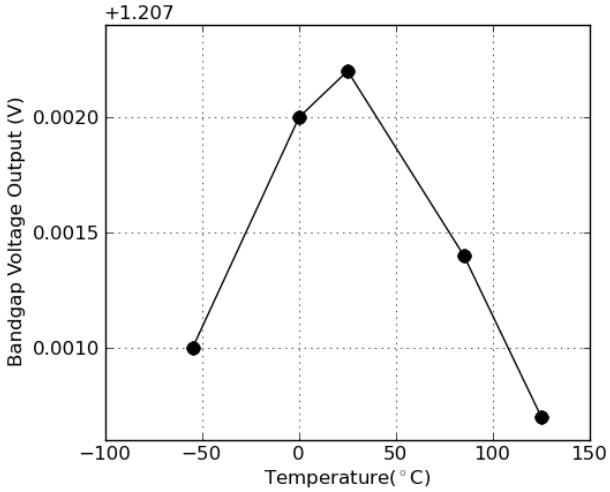


Figure 22: Typical reference voltage versus temperature.

The produced voltage reference is amplified by a selectable factor (x2 amplifier-see section 3.6) before being applied to the ADC. Typical gain curve versus input common mode is shown in Fig. 23.

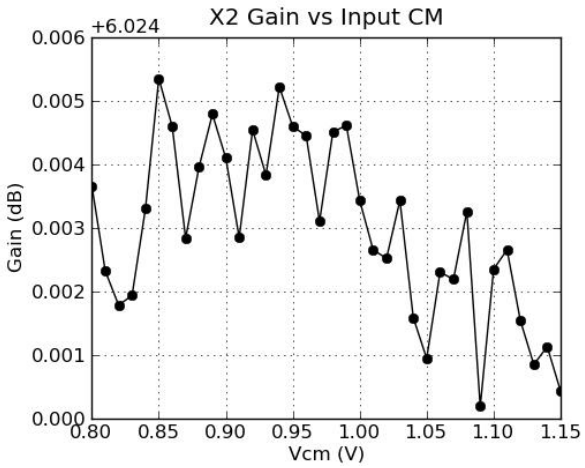


Figure 23: X2 amplifier gain stability versus input common mode.

Power Supply Rejection is 84 dB at DC dropping to 80 dB at 100 KHz.
Input resistance of the amplifier is $>$ 1 GΩ.

10.3 Analog Input Voltage Range

The analog input voltage range is from -0.7 to 3.2 Volts. The full scale range is from 0 to 2.5V (depending on the applied voltage reference). If the user wants to extend the input range two solutions are envisioned:

- **Input scaling with passive components:** This solution is easy to apply and the input range can be extended to any level the user wants. Special care needs to be taken when cross strapping ETM devices and the one is powered off.
- **Input scaling with active components:** This solution requires active components to perform down scaling of input voltages. Cross strapping of ETM devices to the same signal source (with one ETM being powered off) is more straightforward in this case.

10.4 Temperature Measurement

The electrical performance characteristics of the Current Source are listed in table 27.

Table 27: Temperature measurement unit electrical performance characteristics.

Output Resistance (R_{OUT})	$>$	1GΩ
Maximum Output Voltage ($V_{OUT,MAX}$)	$>$	2.4V
Maximum Offset Voltage ($V_{Offset,MAX}$)	$<$	3mV

The user can connect either a PT 1000 or an NTC temperature sensor on the device. In table 28 the temperature resolutions and linearities achieved with the two temperature sensors are shown.

Table 28: Temperature Resolution of the ETM Device.

Temperature Sensor	TC R_C (ppm/°C)	Resolution (°C)	Linearity (°C)
PT1000 Roseemount 118MF1000	10	0.12	0.31
NTC YSI44908	10	3.9	-

10.5 Digital Sampling

10.5.1 Digital Threshold Setting

In Fig. 24 the threshold voltage V_{THR} versus the bias resistor value is shown. The common mode variation of the threshold (due to ground difference between ETM GND and D_{IN-}) is close to 100 mV as shown in Fig. 25.

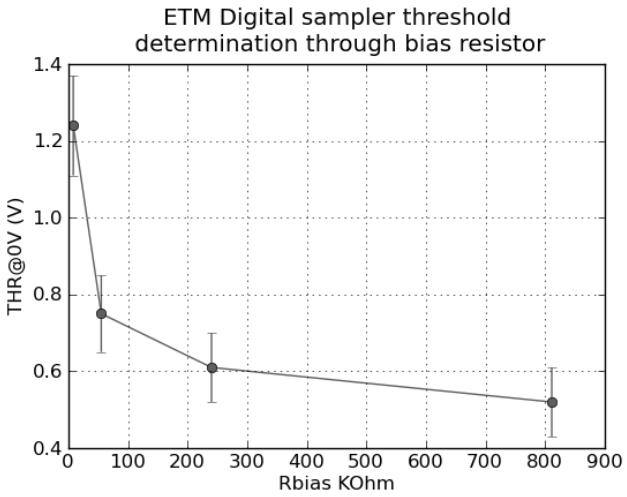


Figure 24: V_{THR} value versus bias resistor value.

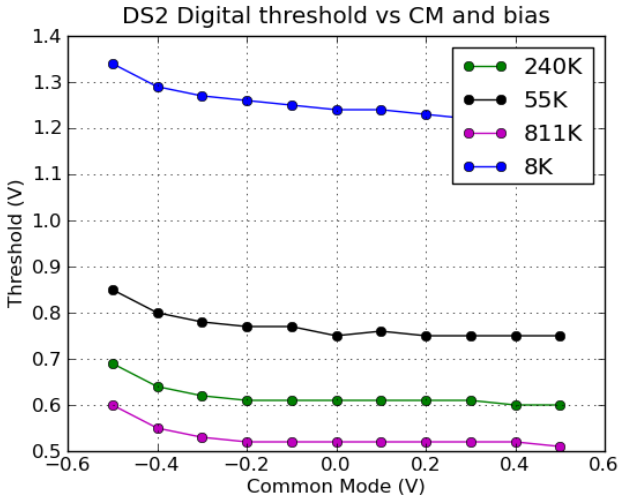


Figure 25: V_{THR} variation due to common mode variation at various threshold settings.

Important Note: Bias resistor values of less than 100 KΩ (resulting to threshold values of 700 mV and above) are advised to avoid SET susceptibility.

10.5.2 Digital Sampler Input Range

The input range of the Digital Sampler inputs is from -0.5 to +3.9 V. If the user wants to extend the input range an external resistive divider can be used. This way input ranges from -1 to 5V can be reached.

10.6 Total Operating Current

The total operating current of the device is shown in table 29. When in RTU mode, extra 0.3 mA are needed due to the fact that the CAN interface is clocked.

When configuring the inputs for temperature measurements, an extra mA is needed for the output current of the Current Source.

Table 29: Operating Current for various configurations. Clock frequency is assumed to be 16 MHz.

Osc	Measurement Type	Configuration	Total Current (mA)
Ext	Voltage Only	STD	2.7
Int	Voltage Only	STD	3.2
Ext	Voltage Only	RTU	3
Ext	Voltage and Temperature	RTU	4
Int	Voltage and Temperature	RTU	4.5

10.7 Operating Current of the Digital Section ($I_{VDD-dig}$) versus Frequency

The digital current of the device (STD mode) versus the master clock frequency is shown in Fig. 26. When the device operates in RTU mode, an extra 1.2 mA needs to be added on top of the curve shown in Fig. 26.

10.8 Total Operating Current (I_{VDD}) versus Temperature

The overall current of the device versus temperature is shown in Fig. 27.

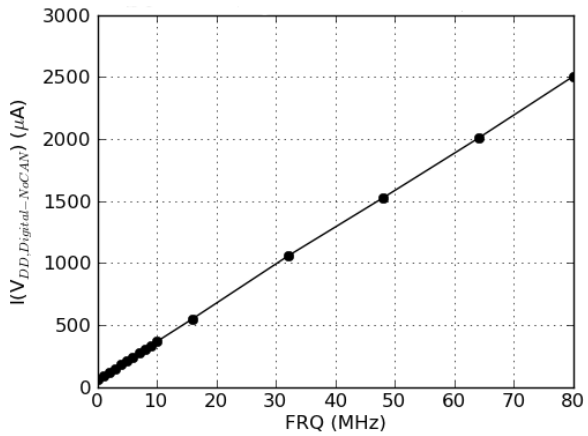


Figure 26: Digital Current versus frequency when in STD mode. When in RTU mode 1.2 mA should be added on top of the curve.

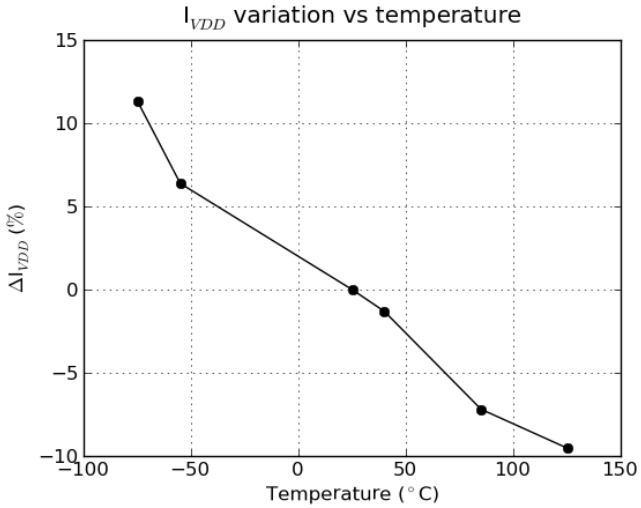


Figure 27: Total current variation versus frequency. The total current decreases as temperature increases. Total variation is $\pm$10%.

10.9 Summary of Electrical Characteristics

The electrical parameters of the ETM, as well as the typical and corner values are listed in Table 30.

Table 30: Electrical characteristics of the ETM device.

Parameter	Conditions	Min.	Typ.	Max.
2.5 V Power Supply (V)		2.25	2.5	2.75
2.5 V Power Supply ripple (Vpp)			20@100KHz	
3.3 V Power Supply (V)		2.97	3.3	3.63
3.3 V Power Supply ripple (Vpp)			20@100KHz	
2.5 V Power Supply Current (mA)			7	10
3.3 V Power Supply Current (mA)			0.7	1
High level Input Voltage V_{IH} (V)		2		
Low level Input Voltage V_{IL} (V)				0.8
Low level Output Voltage V_{OL} (V)	I_{OUT}=1mA			0.31
High level Output Voltage V_{OH} (V)	I_{OUT}=1mA	3.1		
STD Mode Operating Frq. (MHz)			16	24
CSC Mode Operating Frq. (MHz)			16	24
RTU Mode CAN clock Operating Frq. (MHz)		15.7472	16	16.2528
RTU Mode CTU clock Operating Frq. (MHz)		8	16	24
Input Pad Capacitance C_{IN}(pF)		3	5	6
IO Pad Capacitance C_{IO}(pF)		4	6	7
Low Level Input Current I_{IL} (mA)				0.01
High Level Input Current I_{IH} (mA)				0.01
2.5V Stand by Current $I_{STDBY2p5}$ (mA)		3	4	
3.3V Stand by Current $I_{STDBY3p3}$ (mA)			0.2	0.3
Digital Sampler				
Threshold (V)		0.8	0.9	1
Conversion Speed (MHz)			16	24
Channel to Channel threshold variation (mV)			1	2
Threshold drift due to temperature (mV)			$\pm$50	$\pm$75
Threshold drift due to power supply (mV)			$\pm$50	$\pm$75
Threshold drift due to TID (mV)			$\pm$50	$\pm$75
ADC				
Offset (LSB)			0.5	1
DNL (LSB)			0.2	0.5
INL (LSB)			0.5	1
Sampling Rate (KSPS)	at fastest supported Scan Sequence		16	24
Temperature Measurement				
I_{BIAS} (mA)			1	3
$V_{OUT,MAX}$ (mV)		2.4	2.45	2.6
Temperature Variation (nA@1mA output)			5	10
PSRR (dB - to 100KHz)		84	90	
Voltage Reference				
Reference voltage (V)		1.2	1.22	1.225
TC (ppm/°C)			12	25
PSRR (dB - to 100KHz)		84	90	
External reference voltage (V)	X2 amplifier included	0.8		1.25
	Directly to the ADC	0.8		3
X2 Gain (V)	Defined through external resistors		2	2.2
POR Characteristics				
POR Duration (ms)	($C_{POR,Ext}$=40nF from POR to GND)		50	
Digital Timings				
t1 (ns)	see Fig. 28		26	
t2 (ns)	see Fig. 28		16	
t3 (μs)	see Fig. 28		3.875	
t4 (ns)	see Fig. 28		8.5	
t5 (ns)	see Fig. 28		14	
t6 (ns)	see Fig. 28		13	

In Fig. 28 the timing of the PacketWire IF I/Os is shown.

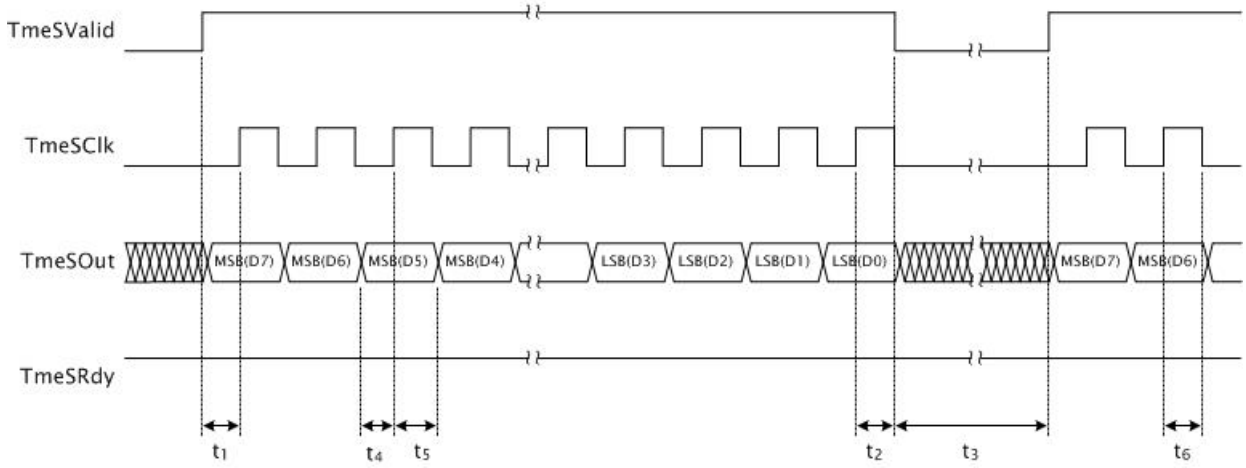


Figure 28: Timing of the PacketWire IF signals.

11 Radiation Performance

11.1 TID

ETM can withstand more of 1Mrad of TID. In table 31 the effects of a TID equal to 1Mrad to the device analog parameters is presented.

Table 31: Summary of TID effects on the analog performance of the ETM ASIC at 1 MRad

Parameter	Drift	Units
Power Supply Regulator Output	4	mV
Voltage Reference Abs. Value	2	mV
Voltage Reference Temp. Coeff	3.5	ppm/°C
ADC INL with ext. reference	±1	LSB
ADC DNLwith ext. reference	0.2	LSB
Temperature Measurement Output Current @ 1mA	10	nA
Digital Sampler threshold	50	mV

The digital section performance is not affected by TID at 1MRad.
The overall operating current increase is negligible.

11.2 SEE

The cross section curves for the ETM device are shown in Fig. 29.
For LET levels up to 67 MeV/mg/cm^2 all the SEUs are expected in the data path.
It should be noted that this cross section corresponds to the slowest sampling rate (2mHz).

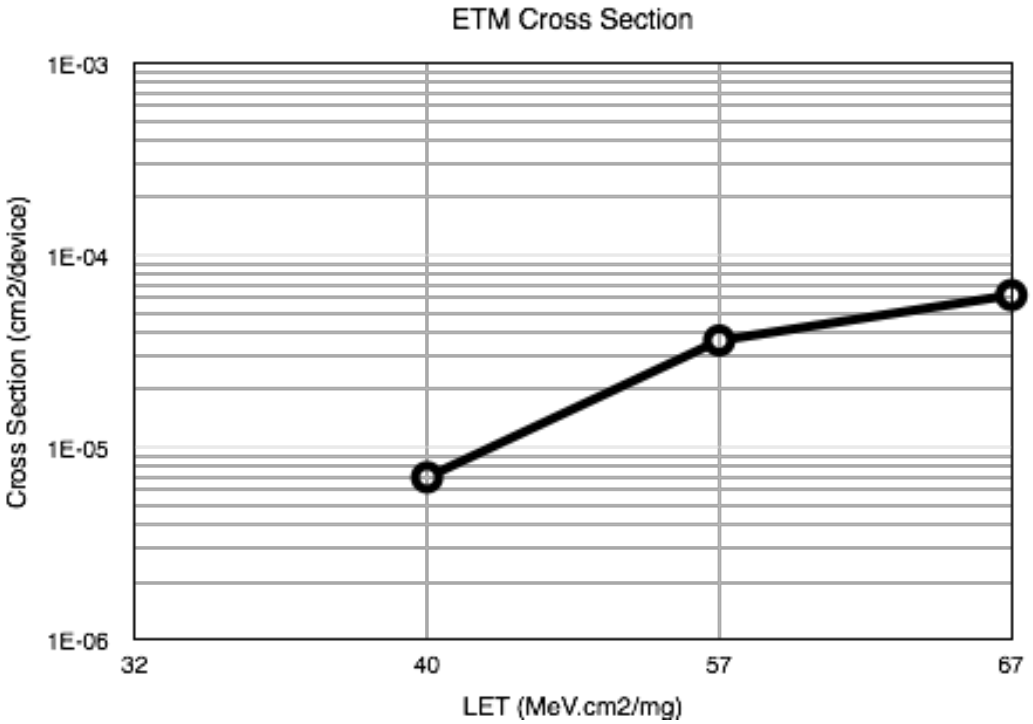


Figure 29: ETM SEU cross section

12 Mechanical Parameters

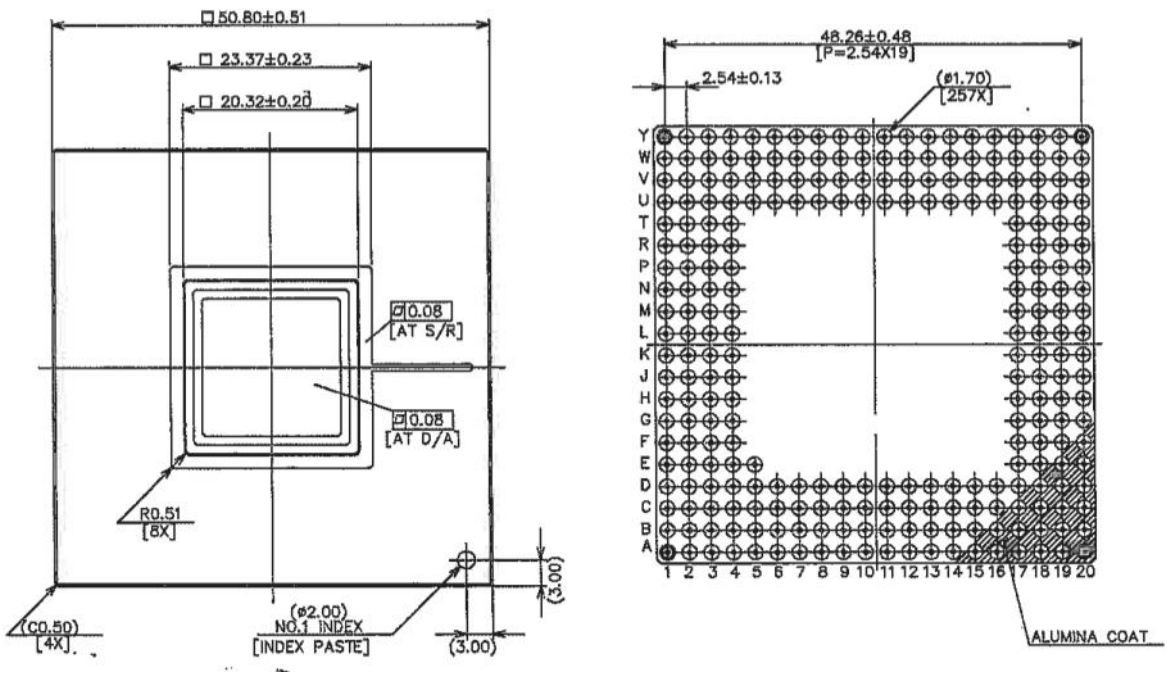
12.1 Package Physical Dimensions

The ETM2 (FM ETM) device is available in two packaging configurations:

- 256 PGA Package
- 256 CQFP Package

12.2 PGA Packaged ETM Devices

The physical package dimensions are shown in Fig. 30.



(a) Top View

(b) Bottom View

Figure 30: FM ETM PGA package physical dimensions (Units:mm)

12.3 CQFP Packaged ETM Devices

The physical package dimensions are shown in Fig. 31.
In order to mount the device to a PCB a ZIF socket shall be used as shown in Fig. 32. As an example the ZIF socket PA-QFJ256SB-P-Z-01 from Ironwood Electronics can be used.

12.3.1 Lid Grounding

The lid of the CQFP package is not electrically connected to the ground.

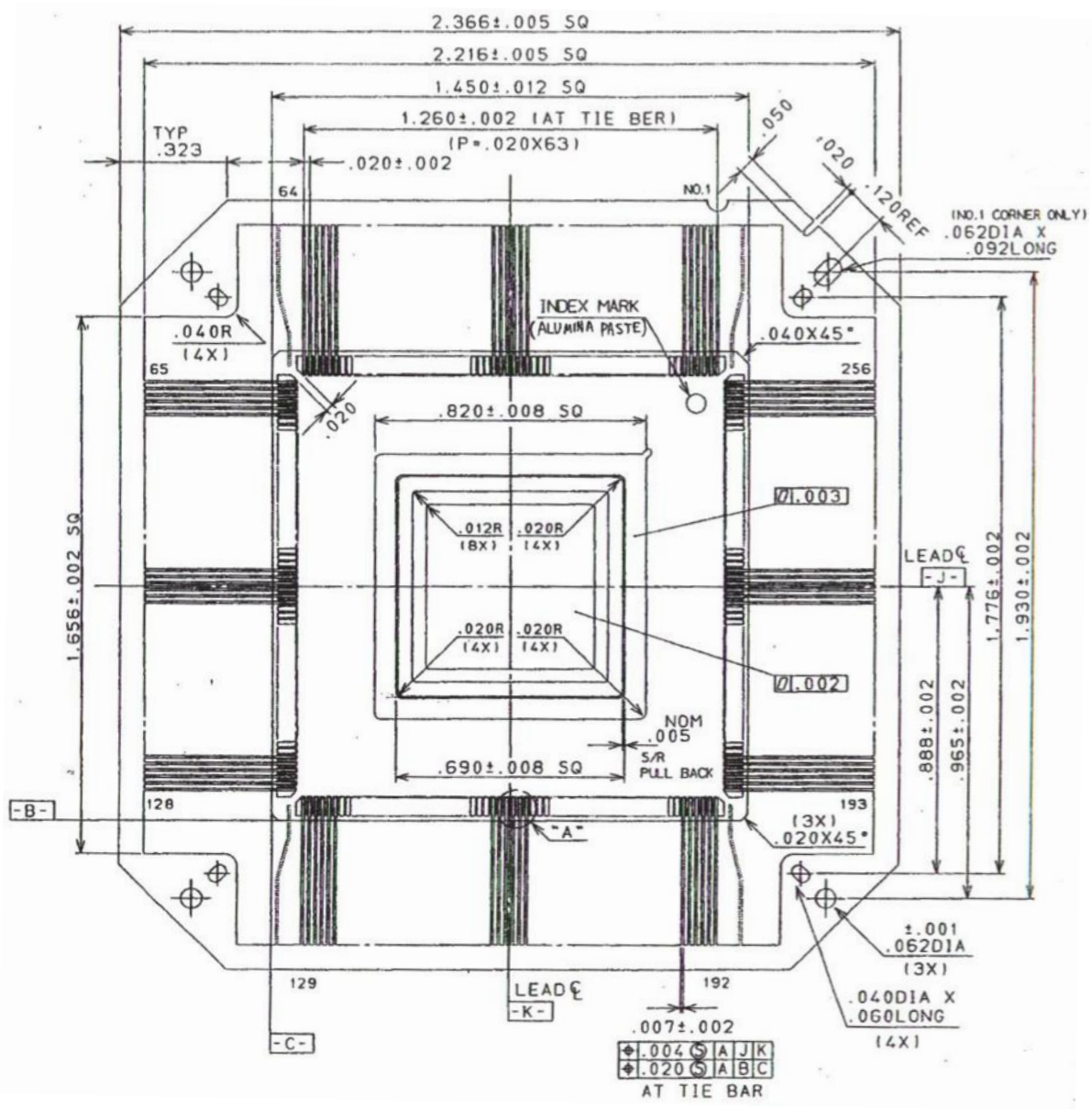
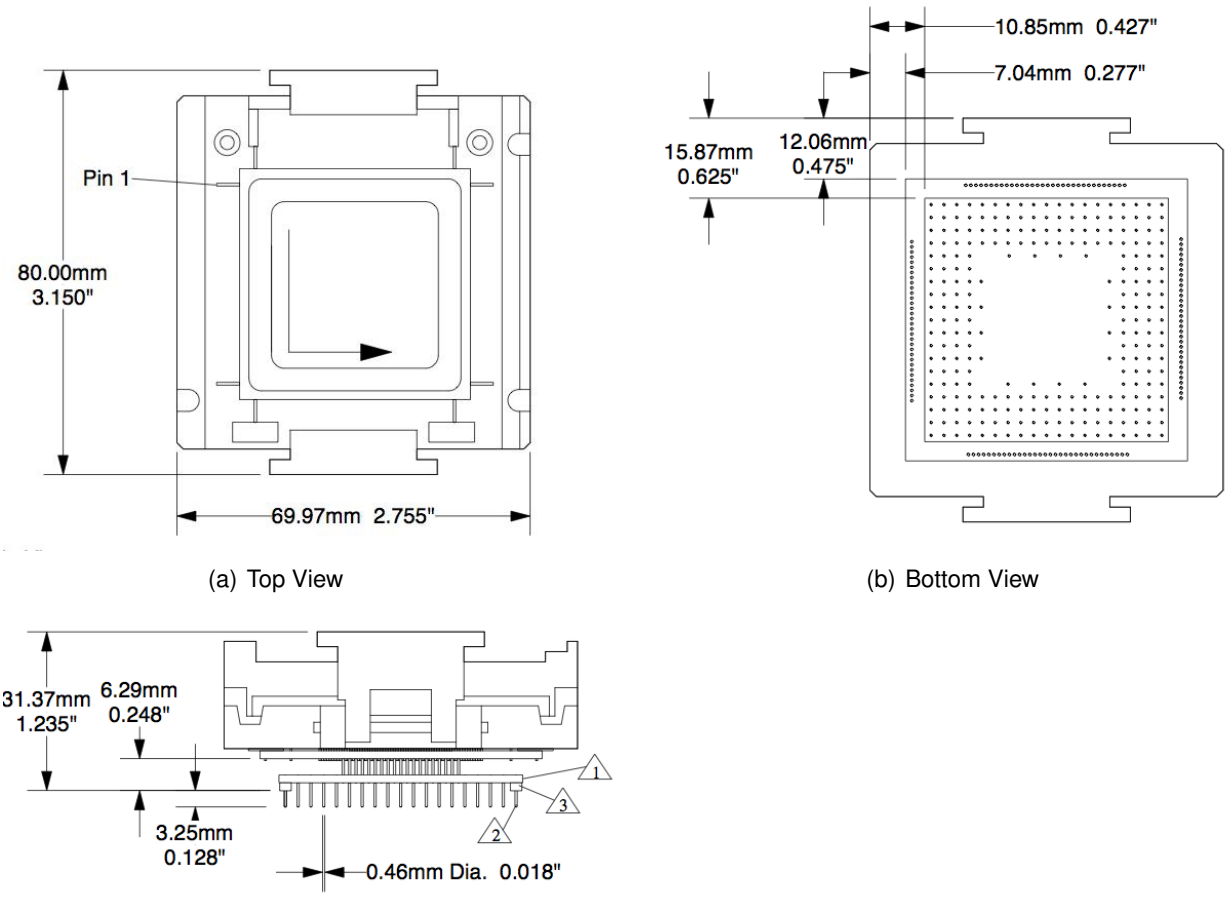


Figure 31: FM ETM CQFP package physical dimensions (Units:inches)



(a) Top View

(b) Bottom View

(c) Side View

Figure 32: ZIF socket used for mounting FM ETM on a PCB.

12.4 Bare Die Dimensions

The size of the bare die is 5289.24 μm x 5289.12 μm.

13 I/Os Functionality

13.1 List of ETM Pins

Table 32: FM ETM IOs Functionality Description.

Pad Name	No of Pads	Comments	I/O
Input Channels Interface Pads			
Din[15..0]+, Din[15..0]-	32	16 Differential Digital Channels Inputs. Input impedance is $>1G\Omega$.	DI
AnChIn[31..0]+, AnChIn[31..0]-	64	32 Differential Analog Channels Inputs. Input impedance is $>1G\Omega$.	AI
CsChOut[31..0]	32	32 Analog Channels Current Source Outputs.	AI/O
Power Supply Pads			
Vdd_2p5An	5	2.5 V power supply input pads for the analog part. When the internal power supply regulator is activated, these pads are used for monitoring purposes.	P
Vdd_2p5Dig	4	2.5 V power supply input pads for the digital part. When the internal power supply regulator is activated, these pads are used for monitoring purposes.	P
Vdd_3p3	5	3.3 V power supply input pads.	P
GND	10	Ground Pads.	P
Configuration Pads			
APID[10..0]	11	Application ID used for the ETM identification.	DI
S_ETM_Conf	1	Select between STD and CSC/DC or RTU operating modes.	DI
S_Sg[1..0]	2	Select how many analog channels (Signals Groups) are active.	DI
S_Conf_Sg01[1..0]	2	Configure conversion mode for Sg0 and Sg1 (Signal Groups 0 and 1).	DI
S_Conf_Sg2[1..0]	2	Configure conversion mode for Sg2 (Signal Group 2).	DI
S_Conf_Sg3[1..0]	2	Configure conversion mode for Sg3 (Signal Group 3).	DI
S_Slave_MasterN	1	Select between Master and Slave configuration in CSC/DC mode. In STD mode has to be fixed Low.	DI
S_Event_NormalN	1	Select between Normal and Event mode.	DI
S_TOS[2..0]	3	Select one of the 6 alternative Time of Origin Stamp (TOS) fields to be included into Space Packets.	DI
S_PackAnIndic	1	Enable Anomaly Indication field inclusion into Space Packets.	DI
S_PackErrCntr	1	Enable Packet Error Control field (CRC) inclusion into Space Packets.	DI
S_Pack_StdSimplN	1	Select between Standard or Simplified Space Packets.	DI
C_iVR[1..0]	2	Control the internal Voltage Regulator.	AI
En_iVR	1	Enable or disable the internal voltage reference.	DI
Vref_iVR	1		AI/O
Vref +,-	2	Used for control and monitor the ADC reference voltage.	AI/O
S_DAZ	1	Select if digital auto-zeroing is performed on the ADC (to be used only in high radiation environment).	DI
S_MClk_In_ExtN	1	Select between internal and external Master clock source.	DI
S_SysClk	1	Select between high and low sampling frequencies (system clock).	DI
S_ScSq_Per[4..0]	5	Define the Scan Sequence Period.	DI
Analog Control Pads			
VBE[2..1]	2	Used for trimming the voltage reference performance.	AI
BG_Vout	1	Used to monitor the performance of the internal voltage reference and to apply an external reference when the internal is deactivated.	AI/O
X2_Bias	1	Bias for the amplification unit of the voltage reference subsystem.	AI/O
psF_Bias	1		AI/O
Bias_CS	1		AI/O
Bias_iVR	1		AI/O
X2_V-	1	Monitoring Pad.	AI
X2_Out	1	Amplified voltage reference output pad. Connect this pad to pad Vref+ in case the internal voltage reference is used.	AO
Cs_V+	1	Connect a resistive divider from pad X2_Out to this pad.	AI
			Cont. –

– Cont.			
Pad Name	**No of Pads**	**Comments**	**I/O**
CS_RC	1	Used to connect the low TC resistor for temperature measurements. Connect a low TC resistor from this pad to pad X2_Out.	AI/O
X2_V+	1	Used for testing the performance of the voltage reference amplification unit. In addition it can be used for applying an external voltage reference to the device.	AI/O
Clock Pads			
MClk	1	Master Clock Input.	DI
CANIF_Clk	1	CAN IF Independent Clock Input (used when the CAN IF is clocked independently from the rest digital part of the ETM which is always clocked by the Master Clock).	DI
IntOsc_MClk	1	Internal Clock Oscillator generated clock (Master Clock).	DO
C-Clk	1	Define the Clock Frequency generated by the Internal Clock Oscillator.	AI/O
Reset Pads			
POR	1	Monitor and control the POR circuitry.	AI/O
MrExtN	1	Master Reset of the whole device.	DI
Communication Interfaces Pads			
CAN_TxD	1	CAN Data Transmit (Output).	DO
CAN_RxD	1	CAN Data Receive (Input).	DI
S_PW/CAN_br[1..0]	2	Set the selected PW / CAN IF supported baud rate.	DI
PW_TmeSOut	1	PW Serial Data Output (through on-chip tri-state driver) connected to SCTMTC VC TmeSIn Input.	DOtri
PW_TmeSClk	1	PW Serial IF Clock Output (through on-chip tri-state driver) connected to SCTMTC VC TmeSClk Input.	DOtri
PW_TmeSValid	1	PW Serial If Data Valid Output (through on-chip tri-state driver) connected to SCTMTC VC TmeSValid Input.	DOtri
PW_TmeSRdy	1	PW Virtual Channel Ready Input (connected to SCTMTC VC TmeSRdy Output).	DI
PW_Bus_GrantOut	1	Used by the PW IF arbitration logic of ETM in CSC/DC mode.	DO
PW_Bus_GrantIn	1	Used by the PW IF arbitration logic of ETM in CSC/DC mode. In STD mode has to be fixed High.	DI
TmStr/ S_CANIF_Clk_Ext_InN	1	Used as Time Strobe Input in STD and CSC/DC modes and as control/ configuration input that selects the CAN_IF's Clock (MClk when '0' or CANIF_Clk when '1') in RTU mode.	DI
Scan Sequence Control/Status Pads			
ScSeqEn	1	Scan Sequence Enable.	DI
ScSeqRun	1	Scan Sequence Run Indication.	DO
Testability Pads			
T_Hard	1	Used for stuck at fault testing of hard values.	DI
PBus[2..0]	3	Used for Stuck At Fault (SAF) testing of triple voted FFs.	DI
T_Sout	1	Output of shift register used for testing the triple voted FFs.	DO
T_TMR_NormOpN	1	Selects either the testing of the triple voted FFs or the ETM normal operation.	DI
S_TMR_Sh_LdN	1	Used to control the triple voted FFs content load/shift out during their testing.	DI
iEb	1		DI
T_Cs	1	Used for testing the Current Source.	AI/O
BG_V+	1	Used for testing the performance of the Voltage Reference Amplifier.	AI
BG_V-	1	Used for testing the performance of the Voltage Reference Amplifier.	AI
X2_VOut	1	Analog Front END test pad.	AI/O

The pads of the ETM ASIC are categorized (as based on the previous table) as:

- P: Power pads that are used to provide power to the ASIC.
- DI: Digital Input Pad.
- DO: Digital Output Pad.
- DOtri: Digital Output Pad with tri-state capability.
- AI: Analog Input Pad.
- AO: Analog Output Pad.

AI/O: Analog Input/Output Pad.

The block diagram of the digital input pad is shown in Fig. 33.

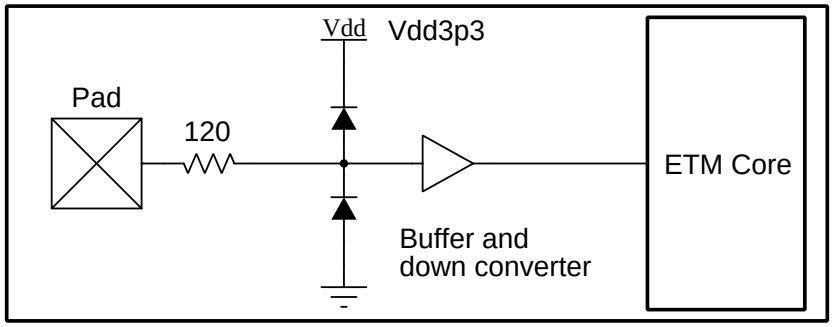


Figure 33: Block diagram of the Digital Input (DI) pad.

The block diagram of the digital output pad is shown in Fig. 34.

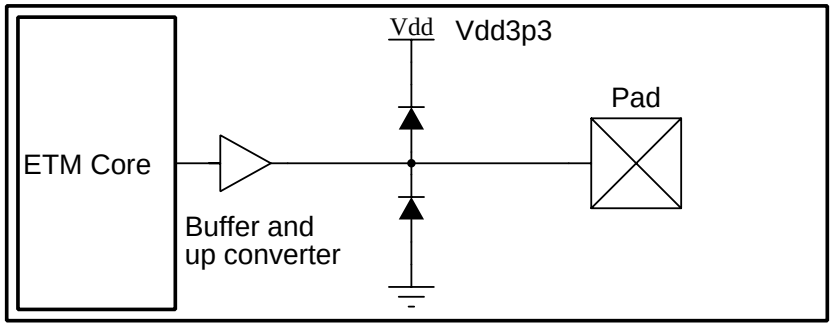


Figure 34: Block diagram of the Digital Output (DO) pad.

The block diagram of the digital output pad with tri-state capability is shown in Fig. 35.

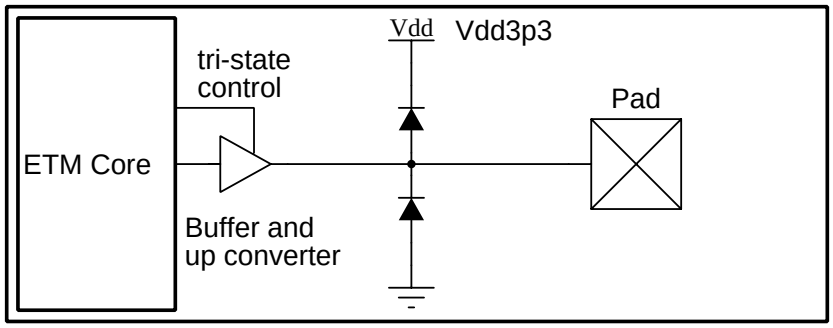


Figure 35: Block diagram of the Digital Output with tri-state capability (DOtri) pad.

The block diagram of the analog pad is shown in Fig. 36. The schematic covers AI, AO and AI/O pads.

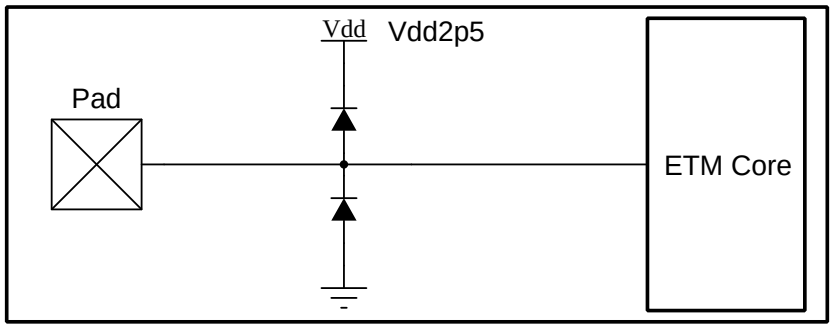


Figure 36: Block diagram of the Analog Input/Output (AI/O) pad.

13.2 Handling of Static Digital Input Pins

All static digital input pins should be connected to either Vdd_3p3 or GND or at an external signal source through a 150 Ω resistor, as shown in Fig.37 since no internal pull up or pull down resistors exist inside the ASIC.

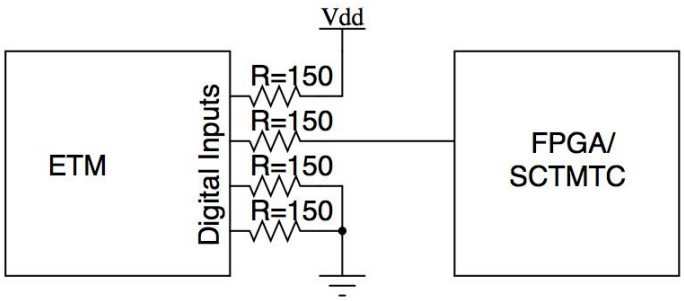


Figure 37: Connections of static digital input pins on the PCB.

14 Cross-Strapping of ETM Devices

In this section information is provided regarding the capability of the ETM to be used for cross strapping of the analog and digital inputs.

14.1 Cross Strapping of ETM Devices for Temperature Measurements

It is possible to use the ETM device for temperature measurements in a redundant scheme as shown in Fig. 38. Two redundant PRTs are used. Each one of the ETM devices uses its own PRT device.

- No electrical connection between the main and redundant ETM devices
- Two separate PRTS are used

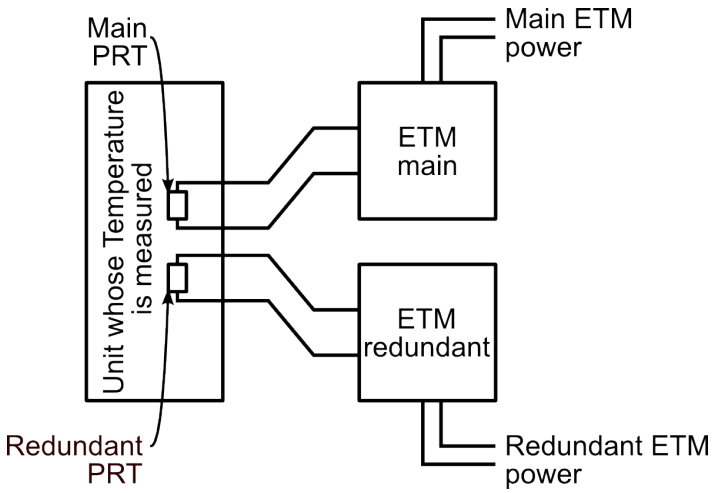


Figure 38: Redundancy scheme for temperature measurements using the ETM device.

14.2 Cross Strapping of ETM Devices for Voltage Measurements

ETMs can be used for voltage measurements in a cross-strapped configuration using external resistors as shown in Fig. 39. It is assumed that the main ETM device is powered-on while the redundant one is powered-off.

- Compatibility with **ECSS-E-ST-50-14C** [D6]
  - $R_{IN,SAMPLING} > 1G\Omega$
  - $R_{IN,NOT-SAMPLING} > 1G\Omega$
  - $R_{IN,POWERED-OFF} > 10K\Omega$
  - C_{IN}=5pF
- Input resistors have to be mounted externally on the PCB
- External resistors do not affect sampling period (250μs to 50s)

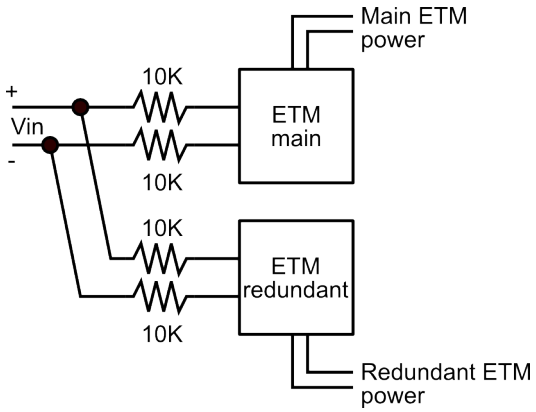


Figure 39: Redundancy scheme for voltage measurements using the ETM device.

14.3 Cross Strapping of ETM Devices for Digital Input Measurements

ETMs can be used for digital input measurements in a cross-strapped configuration using external resistors as shown in Fig. 40. It is assumed that the main ETM device is powered-on while the redundant one is powered-off.

- Compatibility with **ECSS-E-ST-50-14C** [D6]
  - $R_{IN,SAMPLING} > 1G\Omega$
  - $R_{IN,NOT-SAMPLING} > 1G\Omega$
  - $R_{IN,POWERED-OFF} > 10K\Omega$
  - C_{IN}=5pF
- Input resistors have to be mounted externally on the PCB
- External resistors do not affect sampling speed (16 MHz)

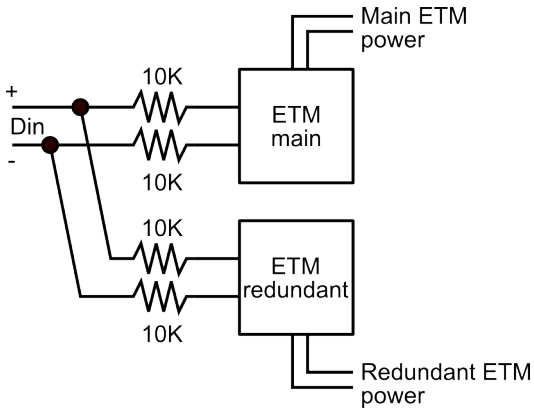


Figure 40: Redundancy scheme for digital measurements using the ETM device.

15 Pins List

Table 33: Terminal connections of the PGA/CQFP (P/C) packaged ETM device.

Lead (P/C)	Pad Name	Lead (P/C)	Pad Name	Lead (P/C)	Pad Name	Lead (P/C)	Pad Name
A1 / 1	NC	Y1 / 65	NC	Y20 / 129	NC	A20 / 193	NC
D4 / 2	NC	U4 / 66	NC	U17 / 130	NC	D17 / 194	NC
C2 / 3	AnChIn7+	W3 / 67	CsChOut0	V19 / 131	Din11+	B18 / 195	T_TMR_NormOpN
D3 / 4	AnChIn7-	V4 / 68	CsChOut1	U18 / 132	Din11-	C17 / 196	APID0
B1 / 5	AnChIn8+	Y2 / 69	CsChOut2	W20 / 133	Din12+	A19 / 197	APID1
E4 / 6	AnChIn8-	U5 / 70	CsChOut3	T17 / 134	Din12-	D16 / 198	APID2
D2 / 7	AnChIn9+	W4 / 71	CsChOut4	U19 / 135	Din13+	B17 / 199	APID3
E3 / 8	AnChIn9-	V5 / 72	CsChOut5	T18 / 136	Din13-	C16 / 200	APID4
C1 / 9	AnChIn10+	Y3 / 73	CsChOut6	V20 / 137	Din14+	A18 / 201	APID5
F4 / 10	AnChIn10-	U6 / 74	CsChOut7	R17 / 138	Din14-	D15 / 202	APID6
E2 / 11	Vdd_3p3	W5 / 75	CsChOut8	T19 / 139	Din15+	B16 / 203	APID7
F3 / 12	Vdd_2p5An	V6 / 76	CsChOut9	R18 / 140	Din15-	C15 / 204	APID8
D1 / 13	GND	Y4 / 77	CsChOut10	U20 / 141	S_SG0	A17 / 205	APID9
G4 / 14	AnChIn11+	U7 / 78	CsChOut11	P17 / 142	S_SG1	D14 / 206	APID10
F2 / 15	AnChIn11-	W6 / 79	CsChOut12	R19 / 143	S_Conf_SG01_0	B15 / 207	S_TOS_0
G3 / 16	AnChIn12+	V7 / 80	CsChOut13	P18 / 144	S_Conf_SG01_1	C14 / 208	S_TOS_1
E1 / 17	AnChIn12-	Y5 / 81	CsChOut14	T20 / 145	S_Conf_SG2_0	A16 / 209	S_TOS_2
H4 / 18	AnChIn13+	U8 / 82	CsChOut15	N17 / 146	S_Conf_SG2_1	D13 / 210	S_Slave_MasterN
G2 / 19	AnChIn13-	W7 / 83	GND	P19 / 147	S_Conf_SG3_0	B14 / 211	S_Event_NormalN
H3 / 20	AnChIn14+	V8 / 84	Vdd_2p5An	N18 / 148	S_Conf_SG3_1	C13 / 212	S_ETM_Conf
F1 / 21	AnChIn14-	Y6 / 85	Cs_RC	R20 / 149	Vdd_2p5D	A15 / 213	GND
J3 / 22	AnChIn15+	V9 / 86	CsChOut16	M18 / 150	GND	C12 / 214	Vdd_2p5D
H2 / 23	AnChIn15-	W8 / 87	CsChOut17	N19 / 151	PW_TmeSClk	B13 / 215	C_iVR1
J4 / 24	AnChIn16+	U9 / 88	CsChOut18	M17 / 152	CANTxD	D12 / 216	C_iVR0
G1 / 25	AnChIn16-	Y7 / 89	CsChOut19	P20 / 153	PW_TmeSOut	A14 / 217	Vref_iVR
J2 / 26	AnChIn17+	W9 / 90	CsChOut20	M19 / 154	CANRxD	B12 / 218	En_iVR
H1 / 27	AnChIn17-	Y8 / 91	CsChOut21	N20 / 155	S_TMR_Sh_LdN	A13 / 219	S_DAZ
K3 / 28	AnChIn18+	V10 / 92	CsChOut22	L18 / 156	IntOsc_MClk	C11 / 220	Bias_iVR
J1 / 29	AnChIn18-	Y9 / 93	CsChOut23	M20 / 157	CANIF_Clk	A12 / 221	T_CS
K4 / 30	AnChIn19+	U10 / 94	CsChOut24	L17 / 158	MClk	D11 / 222	NC
K1 / 31	AnChIn19-	Y10 / 95	CsChOut25	L20 / 159	C_Clk	A11 / 223	NC
K2 / 32	AnChIn20+	W10 / 96	CsChOut26	L19 / 160	GND	B11 / 224	NC
L1 / 33	Vdd_3p3	Y11 / 97	CsChOut27	K20 / 161	Vdd_3p3	A10 / 225	X2_Bias
L2 / 34	Vdd_2p5An	W11 / 98	CsChOut28	K19 / 162	PW_TmeSRdy	B10 / 226	X2_V+
M1 / 35	GND	Y12 / 99	CsChOut29	J20 / 163	PW_TmeSValid	A9 / 227	X2_OUT

Cont. –

– Cont.							
Lead (P/C)	**Pad Name**	**Lead (P/C)**	**Pad Name**	**Lead (P/C)**	**Pad Name**	**Lead (P/C)**	**Pad Name**
L4 / 36	AnChIn20-	U11 / 100	CsChOut30	K17 / 164	PW_Bus_GrantOut	D10 / 228	X2_Vout
N1 / 37	AnChIn21+	Y13 / 101	CsChOut31	H20 / 165	PW_Bus_GrantIn	A8 / 229	X2_V-
L3 / 38	AnChIn21-	V11 / 102	psF_bias	K18 / 166	S_Pack_AnIndic	C10 / 230	Cs_V+
N2 / 39	AnChIn22+	W13 / 103	Din0+	H19 / 167	S_Pack_ErrCntr	B8 / 231	VBE2
M2 / 40	AnChIn22-	W12 / 104	Din0-	J19 / 168	S_Pack_Std_SimpIN	B9 / 232	VBE1
P1 / 41	AnChIn23+	Y14 / 105	Din1+	G20 / 169	S_SysClk	A7 / 233	BG_V+
M4 / 42	AnChIn23-	U12 / 106	Din1-	J17 / 170	S_ScSqPer_0	D9 / 234	BG_Vout
P2 / 43	AnChIn24+	W14 / 107	Din2+	G19 / 171	S_ScSqPer_1	B7 / 235	BG_V-
M3 / 44	AnChIn24-	V12 / 108	Din2-	J18 / 172	S_ScSqPer_2	C9 / 236	iEb
R1 / 45	AnChIn25+-	Y15 / 109	GND	F20 / 173	S_ScSqPer_3	A6 / 237	AnChIn0+
N3 / 46	AnChIn25-	V13 / 110	Vdd_2p5D	H18 / 174	S_ScSqPer_4	C8 / 238	AnChIn0-
R2 / 47	AnChIn26+	W15 / 111	Din3+	F19 / 175	Vdd_2p5D	B6 / 239	AnChIn1+
N4 / 48	AnChIn26-	U13 / 112	Din3-	H17 / 176	GND	D8 / 240	AnChIn1-
T1 / 49	AnChIn27+	Y16 / 113	Din4+	E20 / 177	Vdd_3p3	A5 / 241	AnChIn2+
P3 / 50	AnChIn27-	V14 / 114	Din4-	G18 / 178	S_MClk_In_ExtN	C7 / 242	AnChIn2-
T2 / 51	AnChIn28+	W16 / 115	Din5+	E19 / 179	POR	B5 / 243	AnChIn3+
R3 / 52	Vdd_3p3	V15 / 116	Din5-	F18 / 180	MrExtN	C6 / 244	AnChIn3-
U1 / 53	Vdd_2p5An	Y17 / 117	Din6+	D20 / 181	S_PW/CAN_br0	A4 / 245	Vref-
P4 / 54	GND	U14 / 118	Din6-	G17 / 182	S_PW/CAN_br1	D7 / 246	Vref+
U2 / 55	AnChIn28-	W17 / 119	Din7+	D19 / 183	TmStr/ S_CANIF_Clk_Ext_InN	B4 / 247	GND
T3 / 56	AnChIn29+	V16 / 120	Din7-	E18 / 184	ScSeqEn	C5 / 248	Vdd_2p5An
V1 / 57	AnChIn29-	Y18 / 121	Din8+	C20 / 185	ScSeqRun	A3 / 249	AnChIn4+-
R4 / 58	AnChIn30+	U15 / 122	Din8-	F17 / 186	T_Hard	D6 / 250	AnChIn4-
V2 / 59	AnChIn30-	W18 / 123	Din9+	C19 / 187	Pbus0	B3 / 251	AnChIn5+
U3 / 60	AnChIn31+	V17 / 124	Din9-	D18 / 188	Pbus1	C4 / 252	AnChIn5-
W1 / 61	AnChIn31-	Y19 / 125	Din10+	B20 / 189	Pbus2	A2 / 253	AnChIn6+
T4 / 62	bias_CS	U16 / 126	Din10-	E17 / 190	T_SOut	D5 / 254	AnChIn6-
W2 / 63	NC	W19 / 127	NC	B19 / 191	NC	B2 / 255	NC
V34 / 64	NC	V18 / 128	NC	C18 / 192	NC	C3 / 256	NC

16 Application Note: 3 ETMs Configured in CSC/DC Operation Mode

This application note describes some considerations needed to be taken into account when using multiple ETM devices in CSC/DC mode to interface with one virtual channel of the SCTMTC ASIC Telemetry encoder. In particular the case of concatenating 3 ETMs will be examined.
All three ETMs must have their input pin S_ETM_Conf set to logic low to operate in CSC/DC mode. Only one out of the three ETMs should be configured as Master by means of hard pins. To do so, set the pin S_Slave_MasterN to logic low. The Master device will be the one to transmit first a Space Packet at the beginning of each scan sequence. The other two devices should set the pin S_Slave_MasterN to logic high (3.3 V). This is depicted in Fig. 41.

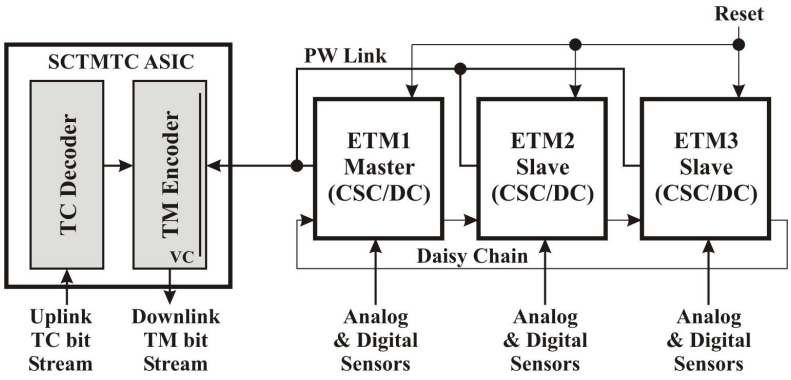


Figure 41: Three ETMs operating in CSC/DC mode in conjunction with SCTMTC ASIC.

The first Slave ETM that is wanted by the user to transmit Space Packets second (after the Master) has to connect its PW_Bus_GrantIn input to the PW_Bus_GrantOut output pin of the Master. Finally, the second Slave ETM has to connect its PW_Bus_GrantIn input to the PW_Bus_GrantOut output pin of the first Slave ETM. The daisy-chain closes by connecting the PW_Bus_GrantIn input of the Master to the PW_Bus_GrantOut output pin of the second Slave ETM, as depicted in Fig. 41.
It is noted again that only one out of the three ETMs should be configured as Master, otherwise physical damage to the ETM devices is possible. The rest of the device settings (e.g. number of active sampling channels) can be independently set per device. It is recommended, however, that the scan sequence period of all cascaded ETMs is set to the same value so as that no packets are lost due asynchronous operation of the devices. Additionally, the Master Reset, Master Clock and ScSeqEn input pins of all cascaded devices have to be connected to the same source.
In particular, concerning the Master Reset input, it is recommended that it is connected to a source that can control it (e.g. a pulse tele-command output of SCTMTC) so that if a problematic behavior is detected (e.g. receiving 2 instead of 3 packets per scan sequence period) there will be the possibility to reset and re-initialize the ETMs. This is not necessary in STD mode.

16.1 Handling of Test Inputs

Some input pins are meant for test purposes and are not used during nominal operation. Table 34 indicates what voltage should be applied to these signals during nominal operation.

Table 34: Test pins necessary connections during nominal operation.

Pad name	Voltage for Nominal Operation
T_Hard	0 Volt
PBus0	3.3 Volt
PBus1	3.3 Volt
PBus2	3.3 Volt
T_TMR_NormOpN	0 Volt