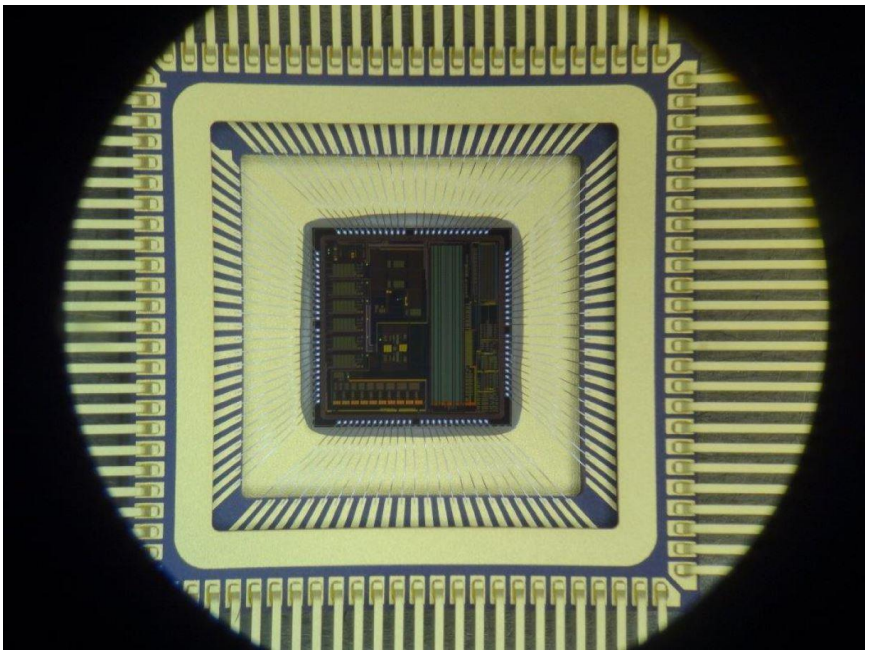
FINAL REPORT

“Qualification of a 14-bit ADC ASIC for Pressure Sensors”

ESA/ESTEC Contract No. 4000113084/14/NL/LF

Document Designation: D_FM-SIF4_QUAL_3.2_FR



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ESA STUDY CONTRACT REPORT

ESA Contract No: *4000113084/14/NL/LF*	SUBJECT: Qualification of a 14-bit ADC ASIC for Pressure Sensors	CONTRACTOR: SPACE-ASICS S.A.
* ESA CR( )No:	No. of Volumes: 1 This is Volume No: 1	CONTRACTOR'S REFERENCE : D_FM-SIF4_QUAL_3.2_FR

ABSTRACT:

The Generic Sensor Interface (SIF4) ASIC is a Rad-Hard, low-power, mixed signal analog digital device, developed by SPACE-ASICS and DUTH/SRL to perform all the functions needed for interfacing with various strain gauge type of sensors that measure: Pressure, Displacement, High-precision single-ended Voltage measurements and Housekeeping in space instrumentation. The SIF4 ASIC is able to provide sensor biasing with constant current and includes built-in Instrumentation Amplifier, signal quantization with a 14-bit ADC, rad-hard Voltage Reference and I2C and SPI Interfaces for data transmission to a micro-controller.

The SIF4 ASIC has the capability to interface up to 6 Sensors and measure up to 8 Single Ended (SE) signals. The device can also be used for Temperature Measurements in 12 channels.

The SIF4-ASIC was fabricated in TSMC 0.25 μm CMOS MS Technology and assembled in CQFP100 packages.

Under the present contract, a Lot Evaluation Campaign was performed on the FM SIF4 devices, which included: SEM Inspection, Acceptance Electrical Tests (ICO, SAF, IDDQ, Functional and Thermal tests), ESD tests, Radiation TID tests (SIF4 can withstand more than 800 Krad of TID), Radiation SEE tests (SIF4 is immune to SEL and SEFI up to at least an LET level of 81.6 MeV/mg/cm2 and SEU free up to an LET of 52.9 MeV/mg/cm2), Screening Tests (High Temperature Stabilization Bake, Temperature Cycling, PIND, Power Burn-in, High & Low Temperature Electrical Measurements, Room Temperature Electrical Measurements, Seal Tests, External Visual Inspection and Solderability Test) and Lot Validation Tests according to ESCC9000 (Mechanical Subgroup Tests, Environmental subgroup Tests, Endurance Subgroup Test, Assembly Capability Subgroup Tests).

The Campaign was completed successfully and a Lot of qualified Rad Hard Generic FM SIF4 devices, which passed the Lot Evaluation Tests, was formed.

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* Sections to be completed by ESA

** Information to be provided by ESA Study Manager

Contents

Abbreviations

ADC	Analog to Digital Converter
AFEND	Analog Front End
ALTER	ALTER Technology TUV NORD
ASIC	Application Specific Integrated Circuit
DAZ	Digital Autozeroing Algorithm
DUTH/SRL	Democritus U. of Thrace / Space Research Lab
EM	Engineering Model
ESA	European Space Agency
FM	Flight Model
FPGA	Field-Programmable Gate Array
HCM	HCM.SYSTREL Groupe SERMA
ICO	Initial Check Out
IDDQ	Quiescent Power Supply Current
I2C	Inter-Integrate Circuit serial interface
ISB	Inactive Sensor Bias Unit
LET	Linear Energy Transfer
LVS	Layout Versus Schematic
NTC	Negative Temperature Coefficient Sensor
PGA	Programmable Gain Amplifier
POR	Power On Reset
pSIF	Pressure Sensor Interface
PT	Pressure Transducer
PTC	Positive Temperature Coefficient Sensor
RADFET	Radiation sensing Field Effect Transistor
SA	SPACE-ASICS S.A.
SAF	Stuck At Fault
SEE	Single Event Effects
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch up
SEU	Single Event Upset
SPI	Serial Peripheral Interface
TID	Total Ionization Dose

SIF4-QUAL FINAL REPORT

1. Overview

The Final Report summarizes the key activities and results of the Qualification Campaign for the Lot Evaluation Acceptance Tests of the Generic Sensor Interface FM ASICs (FM SIF4 ASICs) undertaken by SPACE-ASICS S.A. under ESA/ESTEC Contract No. 4000113084/14/NL/LF.

1.1 Background Information

The development of a generic 14-bit Analog to Digital Converter (ADC) integrated with Strain Gauge type of Sensors is considered to have high strategic relevance for European space industry. It will contribute to make sensors and especially pressure sensors deployed in space lighter, more accurate and reliable.

As part of the ESA-coordinated General Support Technology Programme (GSTP) the Agency supported the **Development of a 14-bit ADC ASIC for Pressure Sensors (pSIF ASIC)** by the Space Research Laboratory of the Democritus University of Thrace (DUTH/SRL) and SPACE-ASICS S.A. This development support was intended to foster European autonomy as well as industrial competitiveness regarding the spacecraft equipment world market and to render the European aerospace industry independent from the need to purchase components originating from non-ESA Member States.

The SIF4 ASIC development successfully solved several integrated (VLSI) design issues for proper electrical operation and strict space qualification including: high performance, low power, mixed signal cross talk, substrate noise, auto-zeroing techniques, design for testability, latch-up, radiation hardness to total ionizing dose and single event effects.

1.2 Objectives

The objective of the present activity was to manufacture and qualify a Flight Model (FM) of a Digital Interface ASIC to be integrated with a variety of Strain Gauge type Sensors for space applications.

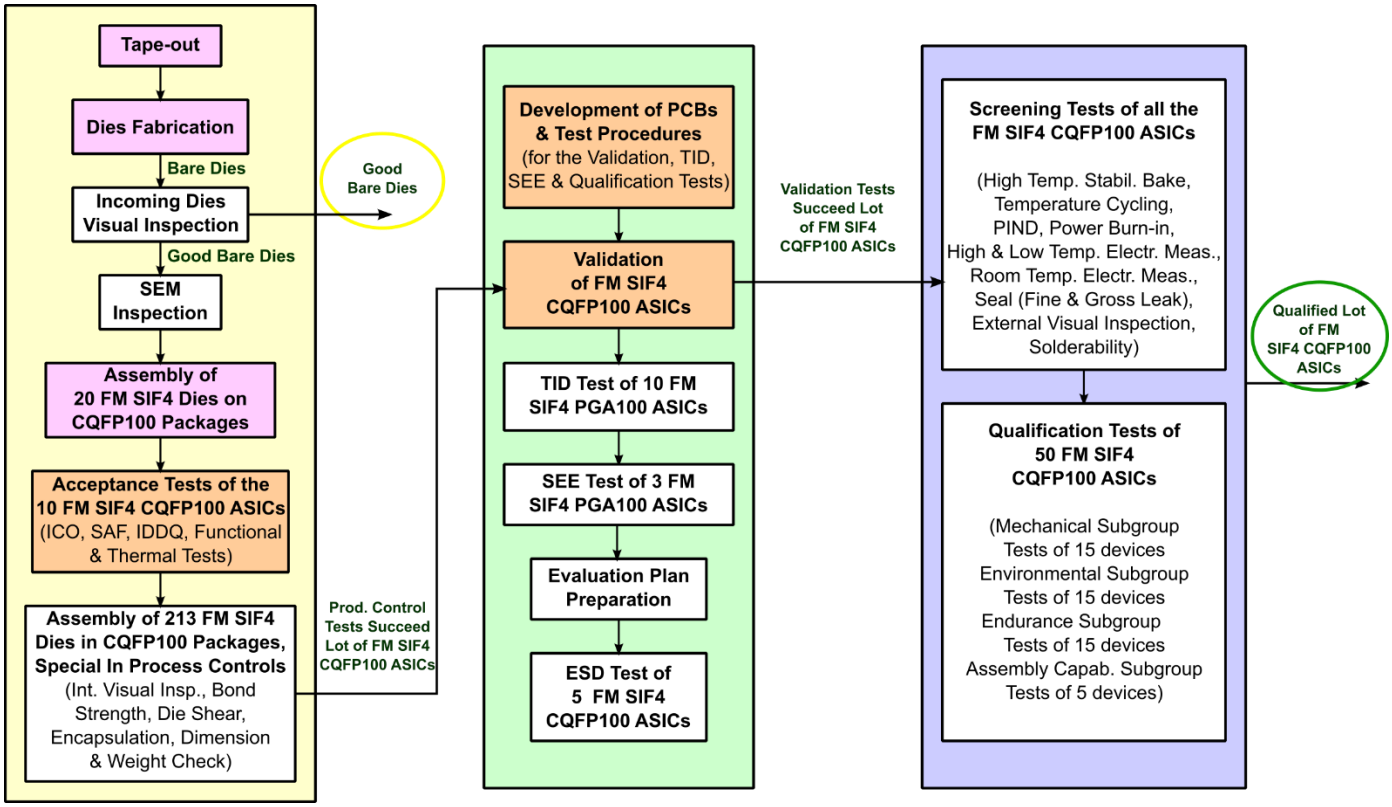
The Outline of the activity is shown in the below Figure:

2. SIF4 Fabrication & Test Preparation

A summary of the key fabrication and test activities undertaken and completed under the project are given below:

2.1 Fabrication and Assembly

- Generation of the Layout and the GDS file
- Submission of the GDS for fabrication in the TSMC 0.25 μm CMOS Process
- Selection through trade-off analysis of a Kyocera CQFP100 Package
- Assembly, Inspection and Special in Process Control of the SIF4 devices by HCM
- SEM Inspection by ALTER



Outline of the FM SIF4 ASIC Lot Evaluation Campaign

2.2 SIF4 Production Test Preparation

The following boards were designed and manufactured for testing the SIF4 devices:

- Production Test PCB: For screening the SIF4 devices after fabrication
- Validation PCB: For functional, temperature and power supply tests
- TID Test PCB: For the TID Testing
- SEE Test PCB: For the SEE Testing
- Application PCB: For integration of the SIF4 ASIC with the Bradford PT

In addition, validation software was generated so as to support the corresponding validation activities, namely:

- Production Test SW: For screening, analyzing the SIF4 devices after fabrication
- Validation SW: For functional, temperature and power supply tests
- TID Test SW: For the TID Testing
- SEE Test SW: For the SEE Testing
- Application SW: For integration of the SIF4 ASIC with the PT

3 SIF4 Validation

The SIF4 ASIC has been tested against an established Design Verification Plan.

The Test Flow is presented below:

3.1 Initial Electrical Measurements

- Initial Check Out (ICO)
- Stack at Fault (SAF)
- Quiescent Power Supply Current (IDDQ)
- Functional Tests
- Thermal Tests

These constitute the **Acceptance Tests**, which were performed on a small sample of devices in order to verify the dice production (along with the **SEM inspection**) and proceed with the assembly of the Evaluation Lot.

3.2 Full Electrical Measurements

The devices from the Evaluation Lot were subjected to the Full Electrical Test Campaign as described below:

- Overall Functionality Tests
- Operating Modes verification tests
- Digital Logic tests which include:
  - Reset Handling
  - Register Programming
  - Clock Management
  - Serial Interface tests (I2C, SPI)
- Analog Performance tests:
  - Voltage Reference
  - ADC
  - Sensor Bias Unit
  - Signal Conditioning Unit
  - Sensor Temperature Measurement Unit
- I/O characteristics validation tests
- Power Consumption tests

4. TID Radiation Results

Total Ionizing Dose (TID) tests for the SIF4 ASICs assembled in PGA120 packages were performed at the ESTEC Radiation Facility.

Three (3) SIF4 devices were irradiated at 35 rad/hr up to 9 Krad in order to test for ELDRS effects.

Ten (10) SIF4 devices were irradiated with a dose rate of 0.36 Krad/hr up to a total dose of 470 Krad and continued with a dose rate of 0.8 Krad/hr up to a total dose of 800 Krad. The irradiation was discontinued at the above total dose.

The devices were tested at intermediate increments and it was concluded that they are immune to a TID of at least 800 Krad.

In the following test data from the SIF4 sub-circuits are presented:

Leakage Current Increase vs TID
The leakage current refers to the digital section of the device. It is a measure of off current of the transistors. The increase of the leakage current after a TID of 800 Krad is minimal (of the order of 200 nA) and it does not affect the functionality of the digital section of the device.

Power Supply Regulator
The generated Power supply voltage varied by less than 3 mV without any effect on the operation of the device.
It was verified that the device can work with and without the internal regulator for TID levels up to 800 Krad.

PT Bias Unit
The PT Bias current variation was less than 10 nA up to 500 Krad.
For all the devices, the pre and post TID output impedance is of the order of several MΩ.
The high impedance of the PT Bias Unit is maintained over the entire temperature operating range.
The IV curve is offset by a small amount. The temperature coefficient before and after TID remained the same at 0.5 ppm/^{o}C.

Voltage Reference
The generated Voltage Reference at various TID levels remained the same to within less than 1mV.
The temperature coefficient of the Voltage Reference before and after TID remained the same at ~14 ppm/^{o}C to within ±1 ppm/^{o}C.

The Programmable Gain Amplifier
The gain of the Programmable Gain Amplifier (PGA) varied by less than 0.005 V/V vs TID.
The PGA offset voltage was not changed during the TID tests.

The Temperature Measurement Unit
The pre and post TID output impedance of the Temperature Measurement Unit is the same (>1MΩ). The measurement resolution of the Temperature Measurement Unit is of the order of a few tens of nA.

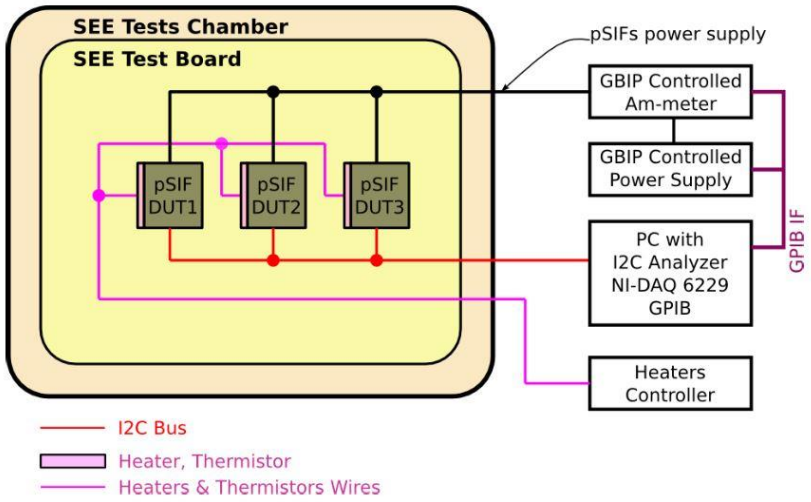
ADC Performance vs TID
For TID levels up to 100 Krad there is no INL shift greater than 1 LSB. For values above 300 Krad, INL shifts start to appear. However, this INL shift is corrected through the Digital Auto-Zeroing algorithm (DAZ).

Digital Section
No loss of functionality was observed in the digital section of the device at 800 Krad.

5. SEE Radiation Test Results

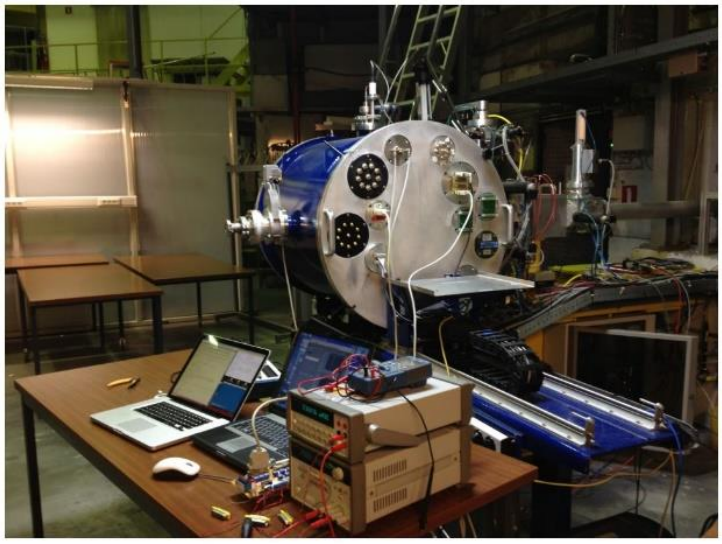
SEE testing of the SIF4 ASIC was performed at the UCL/HIF Heavy Ion Facility in Louvain-La-Neuve (Belgium).

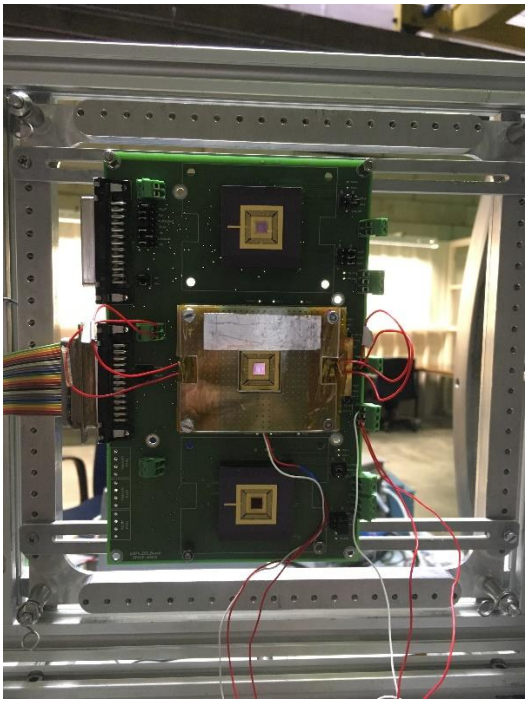
The SIF4 SEE Test setup is shown in the following Schematic:



SIF4 SEE Test setup

The test board housing three (3) unlidded SIF4 devices is shown in the following Figure along with the UCL/HIF Facility.





SIF4 SEE Test Boards at the UCL/HIF Radiation Facility

The characteristics of the ion beams and the selected LET levels are shown in the next Table:

LET ($\frac{MeV cm^2}{mg}$)	Ion type	Tilt Angle (°)	Mean Flux ($\frac{Ions}{cm^2 sec}$)	Reached Fluence ($\frac{Ions}{cm^2}$)	Comments
62.5	$^{124}Xe^{35+}$	0	$2.065 \cdot 10^3$	$1.0002904 \cdot 10^7$	DUT2 Full TP @ 119.4°C
62.5	$^{124}Xe^{35+}$	0	$1.328 \cdot 10^3$	$0.3339295 \cdot 10^7$	DUT1 Full TP
62.5	$^{124}Xe^{35+}$	0	$2.037 \cdot 10^3$	$0.6663978 \cdot 10^7$	DUT3 Full TP
81.6	$^{124}Xe^{35+}$	40	$5.128 \cdot 10^3$	$1.0005468 \cdot 10^7$	DUT2 Full TP@ 119.4°C
45.8	$^{103}Rh^{31+}$	0	$5.203 \cdot 10^3$	$1.0006179 \cdot 10^7$	DUT2 Full TP @ 119.4°C
45.8	$^{103}Rh^{31+}$	0	$5.148 \cdot 10^3$	$1.0008614 \cdot 10^7$	DUT1 Full TP
52.9	$^{103}Rh^{31+}$	30	$5.121 \cdot 10^3$	$1.0006378 \cdot 10^7$	DUT2 Full TP @ 119.4°C
32.4	$^{84}Kr^{25+}$	0	$5.098 \cdot 10^3$	$1.0007566 \cdot 10^7$	DUT2 Full TP@ 119.4°C

LET levels for the SIF4 SEE Test Campaign.

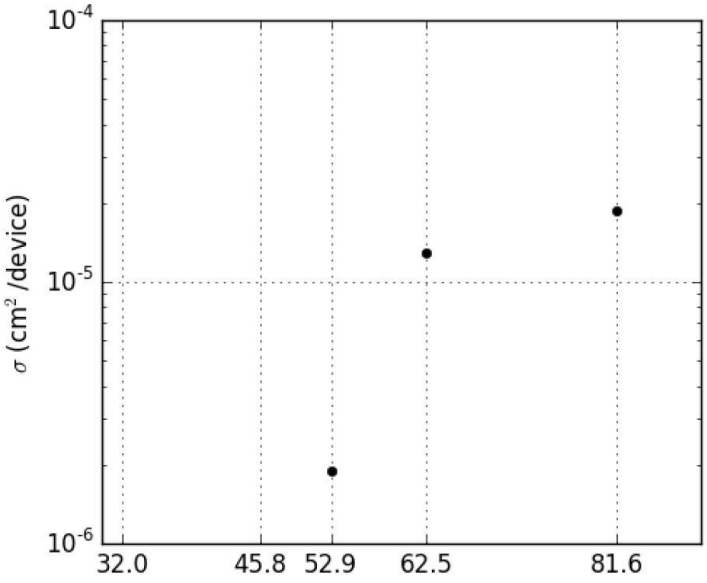
5.1 SEE Test Results Summary

Three (3) devices assembled in PGA120 packages were subjected to SEE tests. The results are summarized in the following table.

Parameter	Value (MeV.cm^2/mg)
SEU Onset	52.9
SEFI	> 81.6
SEL	> 81.6

5.2 SEU Results

The measured SEU cross section of the SIF4 ASIC is shown in the following Figure:



As it can be seen, SEUs start to appear at the LET level of 52.9 MeV.cm^2/mg. Below this level no SEUs were detected. The number of SEUs increases for LET values of 62.5 and 81.6 MeV.cm^2/mg.

5.3 SEFI Results

For all the SIF4 devices and at all LET levels no SEFIs were detected.

5.4 SET Results

No SETs appear as errors in the output code up to an LET threshold of 40 MeV.cm^2/mg

5.5 SEL Results

The devices were monitored for Single Event induced Latch up (SEL) during the entire campaign. Whenever a device was tested, the power supply current was monitored and if the recorded value exceeded the nominal one by a factor of 50%

- an SEL would be recorded
- the power supply would be shut down for the SEL to clear out.

Furthermore, the SIF4 device was heated to 119.4ºC at the LET level of 81.6 MeV.cm2/mg, so as to assess its hardness at elevated temperatures.

The following table shows the LET and fluence levels reached during the SEE test campaign:

LET	Fluence reached for			Temperature	No of SELs
	DUT1	DUT2	DUT3		
$(\frac{MeVcm^2}{mg})$	$(\frac{Ions}{cm^2}) \times 10^7$			°C	0
81.2	>1			119.4	0
62.5	>1			119.4	0
62.5	>0.3		>0.6	ambient	0

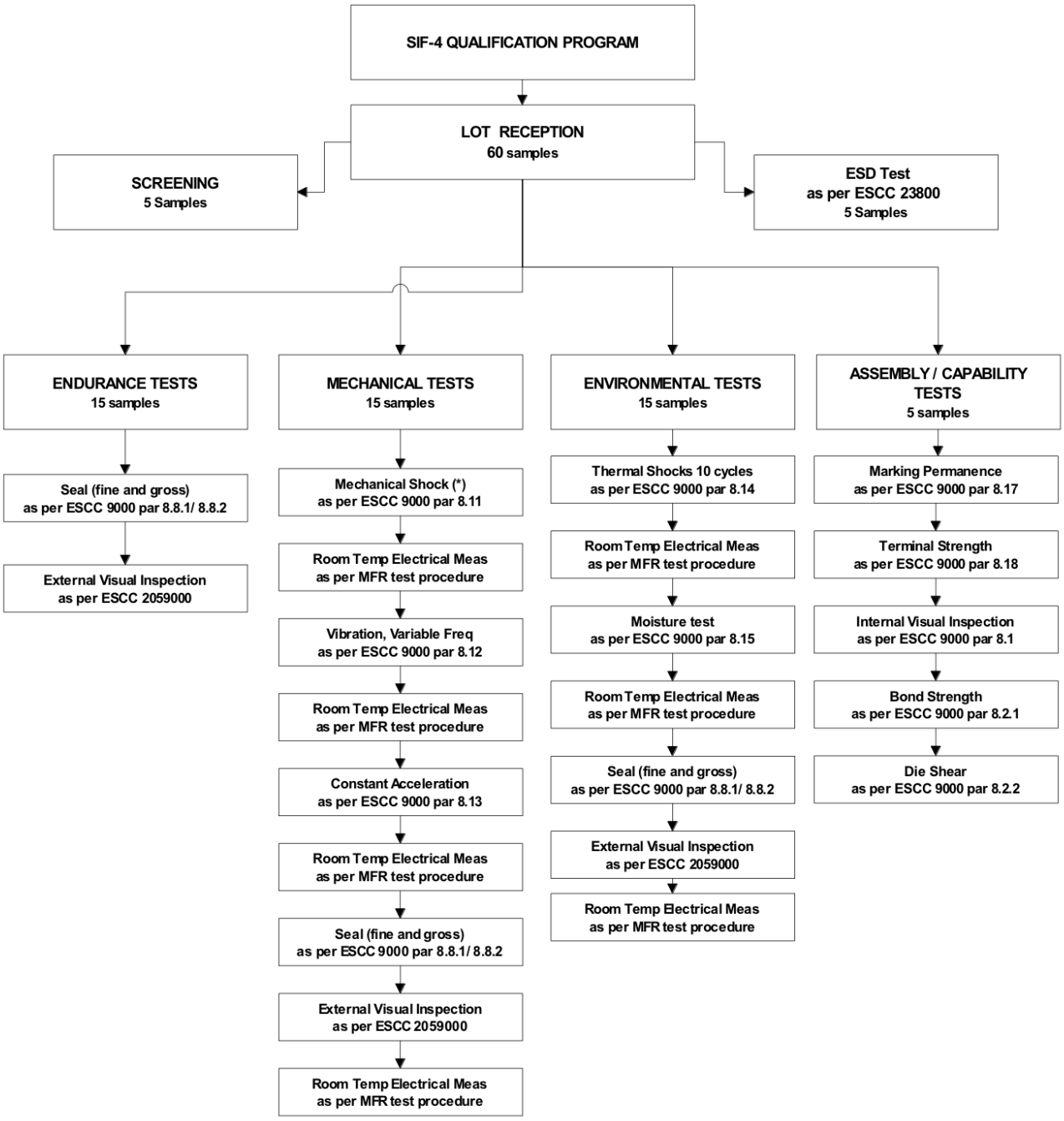
LET and Fluence reached for all three devices.

No SELs were observed for any of the three devices tested up to the highest LET level provided by UCL/HIF.

6 Lot Validation Tests

In this section a summary of the results from the Lot Validation Campaign is presented. Lot Validation Tests were performed at the ALTER facility.

The test flow at ALTER is shown in the Figure below:



6.1 Mechanical Tests

The following Mechanical Subgroup Tests were performed at ALTER on 15 FM SIF4 devices:

- Mechanical shock
- Vibration, variable Frequency
- Constant Acceleration
- Seal (Fine and Gross Leak)
- External Visual Inspection

The SIF4 devices passed successfully the Mechanical Tests and all the intermediate Electrical Tests.

6.2 Environmental Tests

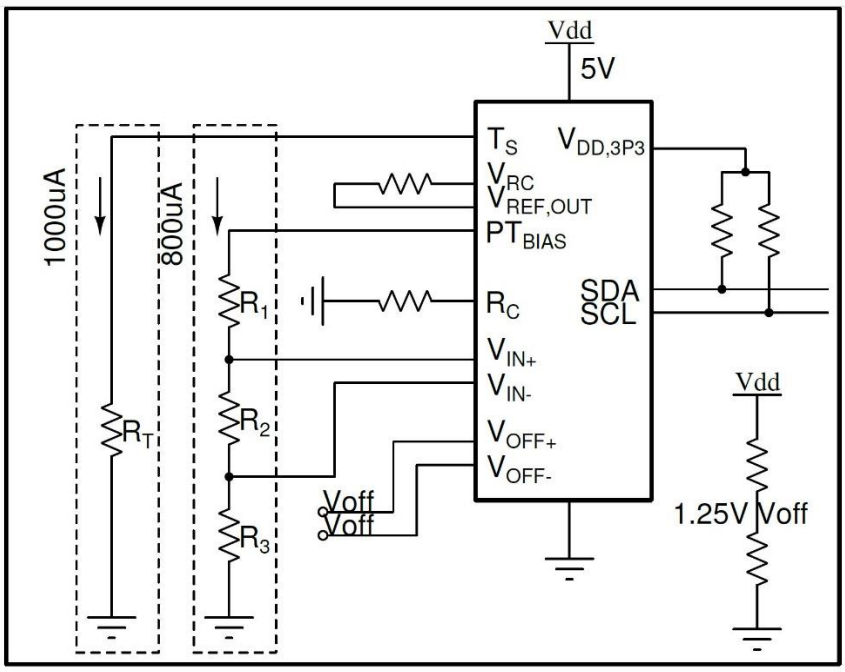
The following Environmental Subgroup Tests were performed at ALTER on 15 FM SIF4 devices:

- Thermal Shocks
- Moisture
- Seal (Fine and Gross Leak)
- External Visual Inspection

The SIF4 devices passed successfully the Environmental Tests and all the intermediate Electrical Tests.

6.3 Endurance Tests

Life Tests were performed at the SPACE-ASICS facility.
During the Life Tests the devices were biased in the configuration shown in the next Figure. The duration of the test was 2000 hrs at 125ºC. During the 2000 hrs only the power supply current of each device was monitored.



Configuration of the SIF4 device during Life Tests

Based on the above, the guaranteed life time of the SIF4 ASIC at various operating temperatures was calculated (from the Arrhenius equation) for two values of activation energy (0.7 and 0.5 eV) and are shown in the Table below:

Temperature (°C)	E_A=0.7 eV		E_A=0.5 eV	
	AF	Guaranteed life (years)	AF	Guaranteed life (years)
25	942.918	215.27	133.23	30.41
35	389.14	88.84	70.80	16.16
45	169.79	38.76	39.15	8.93
55	77.92	17.79	22.44	5.12
65	37.45	8.55	13.30	3.03
75	18.77	4.28	8.12	1.85
85	9.78	2.23	5.09	1.16
95	5.27	1.20	3.28	0.74
105	2.94	0.67	2.16	0.49
115	1.69	0.38	1.45	0.33
125	1	0.22	1	0.22

Guaranteed life of the SIF4 ASIC at various operating temperatures.

The following additional Endurance Subgroup Tests were performed at ALTER on the 15 FM SIF4 devices that past the Life Tests:

- Seal (Fine and Gross Leak)
- External Visual Inspection

The SIF4 devices passed successfully the Environmental Tests and all the intermediate Electrical Tests.

6.4 Assembly Capability Tests

The following Assembly Capability Subgroup Tests were performed at ALTER on 5 FM SIF4 devices:

- Permanence of Marking
- Terminal Strength
- Internal Visual Inspection
- Bond Strength
- Die Shear

The SIF4 devices passed successfully the Assembly Capability Subgroup Tests.

7 ESD Tests

Five (5) SIF4 devices were subjected to ESD tests.
According to ESCC23800 and the obtained results the SIF4 device is classified as ESDS Class 1 with a minimum Critical Path Failure Voltage of 500 Volts.

8. Achievements

8.1 SIF4 Key Functionalities

The generic Sensor InterFace-4 (SIF4) ASIC is capable of interfacing up to 6 Strain Gauge type Sensors (i.e. PTs) and 8 Single Ended (SE) voltage inputs (2 of the 8 SE inputs can be monitored at the same sampling period with the 6 Sensors). In particular, SIF4 is able to:

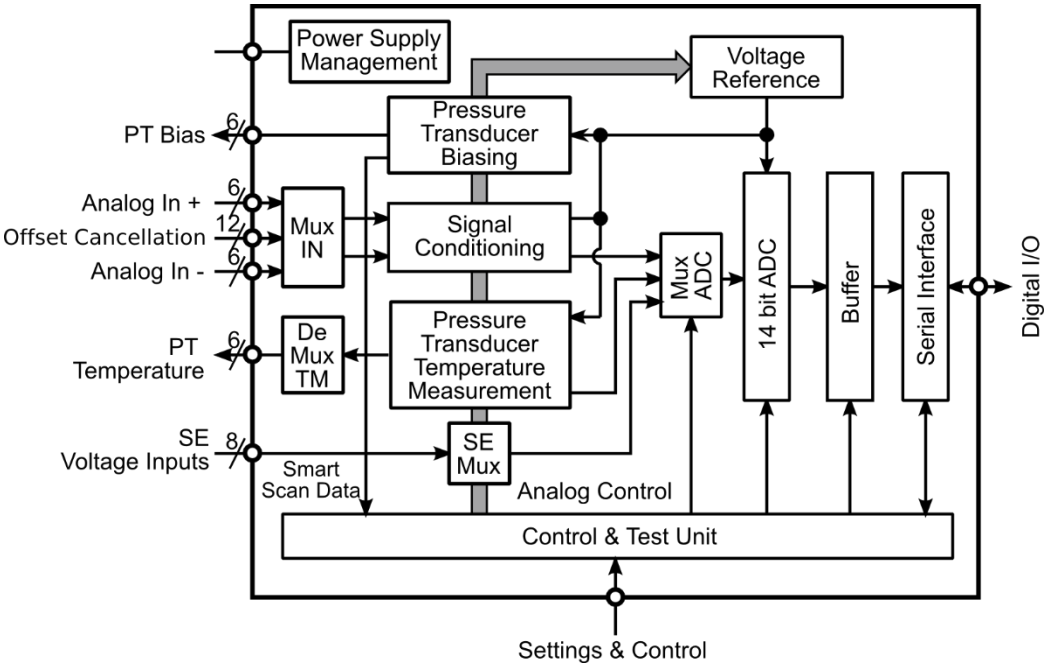
- Bias up to 6 Sensors through a constant current.
- Perform offset cancellation on the Sensor outputs through a programmable input.
- Amplify the differential Sensor voltage of each Sensor to a suitable level for the ADC.
- Measure the temperature on each one of the 6 Sensors.
- Quantize the amplified Sensor voltage, the Sensor Temperature and SE voltages through a 14-bit ADC.
- Format the digitized data into a packet or packets.
- Transmit the quantized data to an external microcontroller through an I2C or SPI bus.
- Receive configuration commands through its I2C or SPI serial interface.
- SIF4 can be configured for operation with:
  - one channel constantly (Fix mode), or
  - scan through the 8 channels (6 Sensors and 2 SEs) sequentially (Scan mode).

8.2 Major SIF4 Subsystems

The SIF4 ASIC consists of:

- A Sensor biasing unit to bias the Sensor(s) with a constant current.
- Current adjustment to fine tune the performance of the Sensor.
- An Inactive Sensor Bias unit (ISB) able to apply a replica current on the inactive sensors in Scan mode so that they remain biased when SIF4 samples another sensor.
- An Analog Front END (AFEND) Multiplexer (MuxIN) to direct the corresponding Sensor (both Sensor outputs and offset cancellation signals) to the Signal Conditioning unit.
- A Sensor Signal Conditioning unit with a Programmable Gain Instrumentation Amplifier (PGIA) with Sensor offset cancellation capability. A T/H function for the input signals before they are applied to the ADC is also implemented by the Signal Conditioning.
- A Voltage Reference Generation unit for Sensor biasing and for the ADC.
- A Temperature Measurement unit to extract temperature information on the Sensor.
- A Demultiplexer (DeMux TM) that directs the Temperature Measurement unit on the Sensor which is currently quantized.
- An Analog Multiplexer (SE Mux) that directs the selected 2 SE input voltages to the ADC.
- A 14-bit ADC along with a Multiplexer (Mux ADC) for feeding the Sensor's temperature or differential voltage into the ADC.
- A Control and Test unit.
- A Data Buffer for temporary storage of the ADC conversions.
- SPI and I2C Interface units for communication with an external microcontroller/ microprocessor.

The High-Level Block Diagram of the SIF4 device is presented in the next Figure:



High-Level Block Diagram of the SIF4 ASIC

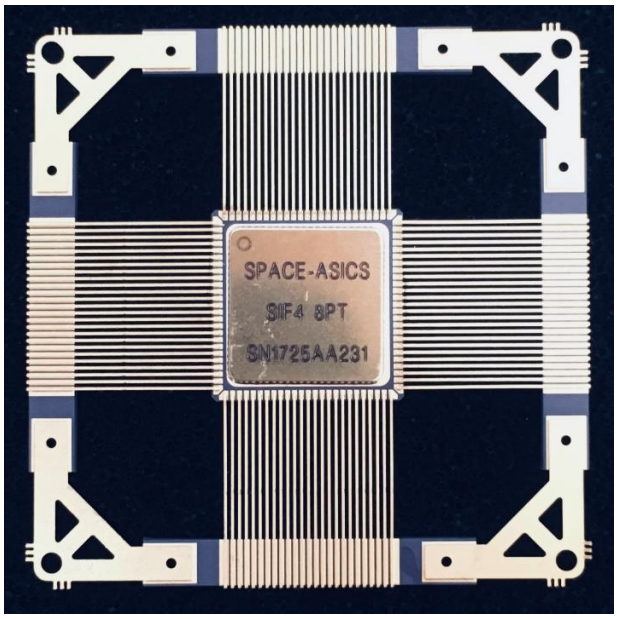
8.3 Key SIF4 Characteristics

The Key SIF4 Characteristics are:

- Fabricated in the TSMC 0.25µm CMOS Technology
- Packaged in CQFP100
- Single power supply 3.3 V (internal voltage regulator)
- Low power consumption (< 30 mW with all 8 channels on and <8 mW with 1 PT on)
- BW limit of input signals to 100 KHz.
- Programmable Gain Differential Amplifier.
- 14-bit ADC (12 true).
- A technology independent Rad-hard Bandgap Reference with a temperature coefficient of < 3 µV/degC @ 1 Mrad
- Wide temperature operating range (-55 to +125 ^{0}C)
- Both PTC & NTC Temperature Sensors supported
- Synchronous/Asynchronous (event driven) sampling
- Various sampling frequencies supported (10, 20, 50 & 100 Ksps)
- Rad-hard to TID > 800 Mrad
- SEL immune to LET > 81.6 MeV.cm2/mg
- SEFI immune to LET > 81.6 MeV.cm2/mg
- SEU free up to LET > 52.9 MeV.cm2/mg

Physical & Mechanical Characteristics

- Die Size = 4930 µm X 4930 µm
- Packaging in CQFP100: POD = 19,05 mm, Cavity: 9,02 mm

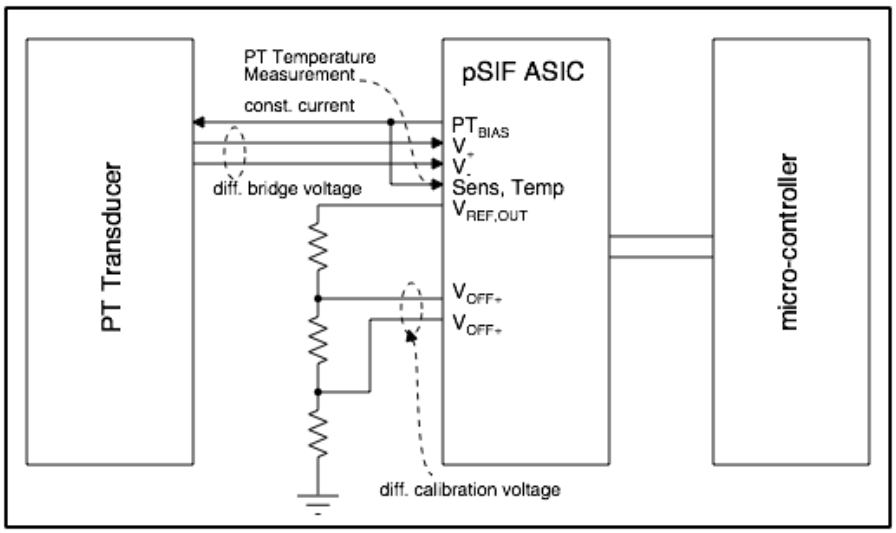


8.4 Key Applications

The SIF4 Applications include:

- Pressure Transducer (PT) Applications
- Other Strain Gauge type of Sensors
- Temperature Measurements with PTC or NTC sensors
- TID Measurements with RADFET

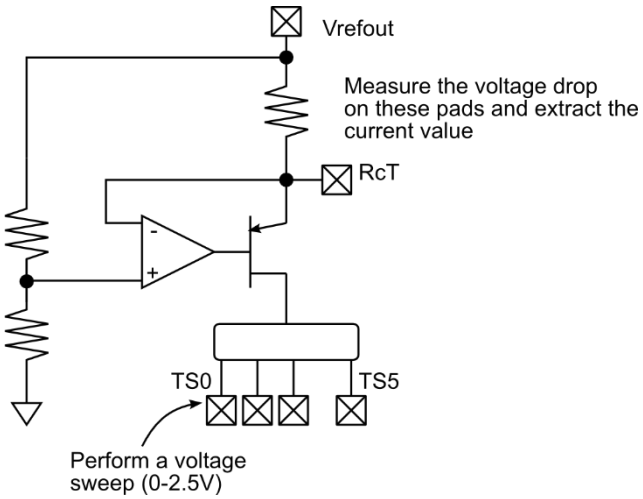
A system Level Block Diagram of the SIF4 device for such Applications is presented in the following Figure:



System Level Block Diagram of the SIF4 ASIC

8.4.1 Temperature Measurements with SIF4

The SIF4 ASIC can be used for temperature measurement applications with Positive Temperature Coefficient (PTC) or Negative Temperature Coefficient (NTC) sensors according to ECSS-E-50-14. In order to perform temperature measurements, the current source is utilized along with a low temperature coefficient external resistor so as to produce an almost temperature independent current. The output current is fed to the sensor and the developed voltage is quantized by the ADC. The setup is shown in the next Figure:



Temperature Measurement Setup

8.4.2 TID Measurements with SIF4

As in the case of temperature measurements, the SIF4 device can be used for TID monitoring through a RADFET. The only difference with the temperature measurement mode is that instead of a temperature sensor, a RADFET is connected at the current source output.

9. Commercialization

The following supply chain was used for the development, manufacturing and testing the SIF4 ASIC:

- Design by SPACE-ASICS S.A.
- Fabrication at the TSMC 0.25μm CMOS Technology.
- The Assembly of the SIF4 dies in CQFP100 Packages is performed by HCM (FR).
- The PCB Test and Application Boards hosting the SIF4 ASICs and the associated circuitry are manufactured at EUROCIRCUITS (Belgium).
- Electrical Characterization of the SIF4 ASICs is performed by SPACE-ASICS and DUTH/SRL.
- Commercialization, Marketing and Selling activities are organized by SPACE-ASICS.

No ITAR restrictions are applicable to the above supply chain. The SIF4 ASIC is available to the European space industry under fair and equal conditions.

10. Follow-up Activities

- SPACE-ASICS is considering the next generation of the SIF4 ASIC, which is envisaged to include a 16-bit ADC.
- SIF4 integration in a variety of users' PT Applications.

11. Conclusions

The Generic pressure Sensor Interface (SIF4) ASIC fabricated and qualified by SPACE-ASICS S.A. under ESA Contract No. 4000113084/14/NL/LF is a mixed signal, low power, rad-hard device capable of interfacing up to 6 Pressure Transducers or other strain-gauge type sensors and up to 8 Single Ended (SE) input voltages, biasing the sensors with a constant current, amplifying the signals with a programmable gain amplifier, measuring the temperature on each one of the sensors, quantizing the amplified voltage through a 14-bit ADC, formatting the digitized data into packets and transmitting the data to an external microcontroller through an I2C or SPI interface.

The FM SIF4 ASIC passed successfully the Lot Evaluation Tests of a Campaign, which included: SEM Inspection, Acceptance Electrical Tests (ICO, SAF, IDDQ, Functional and Thermal tests), ESD tests, Radiation TID tests (SIF4 can withstand more than 800 Krad of TID), Radiation SEE tests (SIF4 is immune to SEL and SEFI up to at least an LET level of 81.6 MeV/mg/cm2 and SEU free up to an LET of 52.9 MeV/mg/cm2), Screening Tests (High Temperature Stabilization Bake, Temperature Cycling, PIND, Power Burn-in, High & Low Temperature Electrical Measurements, Room Temperature Electrical Measurements, Seal Tests, External Visual Inspection and Solderability Test) and Lot Validation Tests according to ESCC9000 (Mechanical Subgroup Tests, Environmental subgroup Tests, Endurance Subgroup Tests, Assembly Capability Subgroup Tests).

Accomplishments

- An all European low-power, rad-hard, mixed signal Analog / Digital ASIC has been designed, fabricated and qualified.
- Expertise was acquired for end-to-end Development and Qualification of mixed signal ASICs for space applications.

12. Documentation

- SIF4 Data Sheet (http://www.space-asics.gr/downloads/SIF4_Data-Sheet_v1C.pdf)