SIF2 Detail Specification

Version	:	V1C
Date	:	August 10, 2015
Classification	:	Confidential
Doc ID	:	SA-SIF2-8.3.5

SPACE ASICS
Apollonos 16 & Patroou 1,
Athens, 10557 Greece
Tel:+30-210-3256993
Fax: +30-210-3256996
Mail: info@space-asics.gr

Table of Contents

Contents

Document Change Note

Version 1A	February 28, 2014	Original Version.
Version 1B	November 19, 2014	Updated after device fabrication.
Version 1C	August 10, 2015	Updated with minor details.

APPLICABLE DOCUMENTS

D1 ESCC Basic Specification No. 21700
D2 ESCC Basic Specification No. 9000
D3 ESCC Total Dose Irradiation Detail Specification No. 22900
D4 ESCC SEE Basic Specification No. 25100

List of Acronyms

ADC	Analog to Digital Converter
AFEND	Analog Front END
ASIC	Application Specific Integrated Circuit
DNL	Differential Non-Linearity
DUTH/SRL	Democritus University of Thrace/Space Research Laboratory
EM	Engineering Model
ESA	European Space Agency
ESD	Electrostatic discharge
FM	Flight Model
HIF	Heavy Ion Irradiation Facility
IA	Instrumentation Amplifier
INL	Integral Non-Linearity
LET	Linear Energy Transfer
MPW	Multi Project Wafer
PCB	Printed Circuit Board
POR	Power On Reset
pSIF	pressure Sensor InterFace
CQFP	Ceramic Quad Flat Package
SAF	Stuck At Fault
SEE	Single Event Effect
SEFI	Single Event Functional Interrupt
SEL	Single Event Latch-up
SET	Single Event Transient
SEU	Single Event Upset
TBC	To be confirmed
TBD	To be determined
TC	Temperature Coefficient
TID	Total Ionizing Dose
TSMC	Taiwan Semiconductor Manufacturing Company
ZIF	Zero Insertion Force

1 General

This document details the ratings, electrical and physical characteristics, test and inspection data of the generic SIF2 ASIC. It also defines the specific requirements for space applications.

1.1 Maximum Ratings

The maximum ratings, which shall not be exceeded at any time during operation or storage, are listed in table 4.

Table 4: Maximum Ratings.

Parameter	**Symbol**	**Max & Min Values**
Supply Voltage	HVV_{DD}	4.5 to 6V
Input Voltage Range	Vin	-1 to 6V
Input Current per Power Pin	I_{INP}	$\pm$50mA
Input/Output Current per Signal Pin	I_{INS}	$\pm$10mA
Operating Temperature Range	T_{OP}	-75 to +135 °C
Storage Temperature Range	T_{STG}	-65 to +150 °C
Soldering Lead Temp. 1.6 mm from case for max 10 s	T_{SOL}	+300 °C
Junction Temperature	T_J	+170 °C

1.2 Recommended Operating Conditions

The recommended operating conditions are listed in table 5.

Table 5: Recommended operating conditions.

Parameter	**Symbol**	**Max & Min Values**
Supply Voltage	HVV_{DD}	4.5 V to 5.6 V dc
Ambient Operating Temperature	T_A	-55 to +125 °C

1.3 Radiation Features

- The device shall not exhibit any performance degradation up to a TID level of 300 KRad (Si).
- The device shall be immune to SELs up to an LET level of 80 MeV/mg/cm^2.
- The device shall be immune to SEFIs up to an LET level of 50 MeV/mg/cm^2.
- No SEUs shall be observed up to an LET level of 50 Mev/mg/cm^2.

1.4 Handling Precautions

Maximum precautions shall be employed for the protection of the SIF2 ASICs from damage by electrostatic discharge during all phases of manufacturing, testing, shipment and any handling.

$$\text{ESD} > 4000 \text{ V (TBC)}$$

2 Mechanical Parameters

2.1 Package Physical Dimensions

2.1.1 48 pin Configuration Package

The physical package dimensions are shown in Fig. 1.

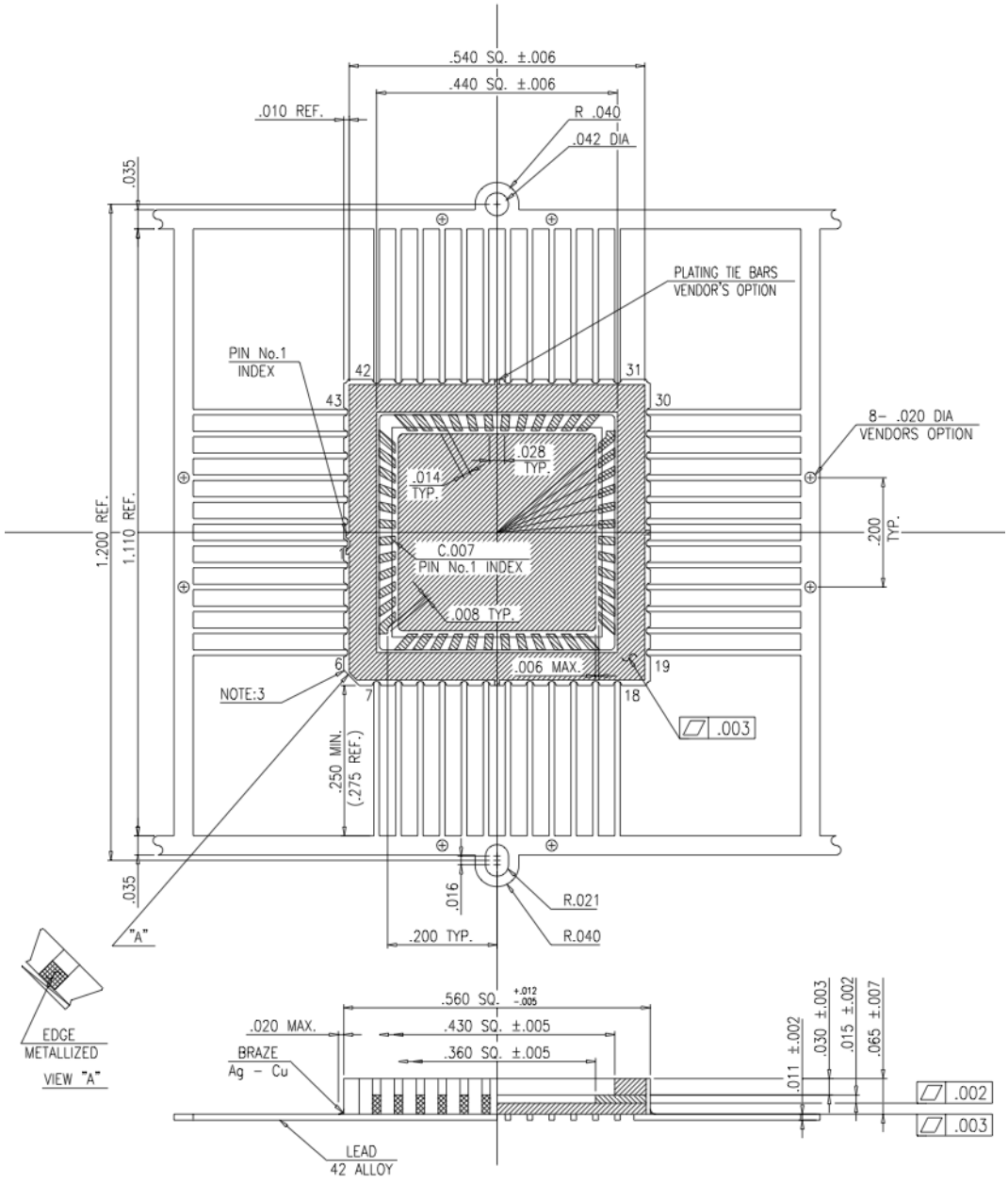

Figure 1: SIF2 package physical dimensions (Units:inches).

2.1.2 100 pin Configuration Package

A 100-pin CQFP package from Kyocera will be used for the flight version of the 8 channel configured SIF2 device. The drawing of the package is shown in Fig. 2.

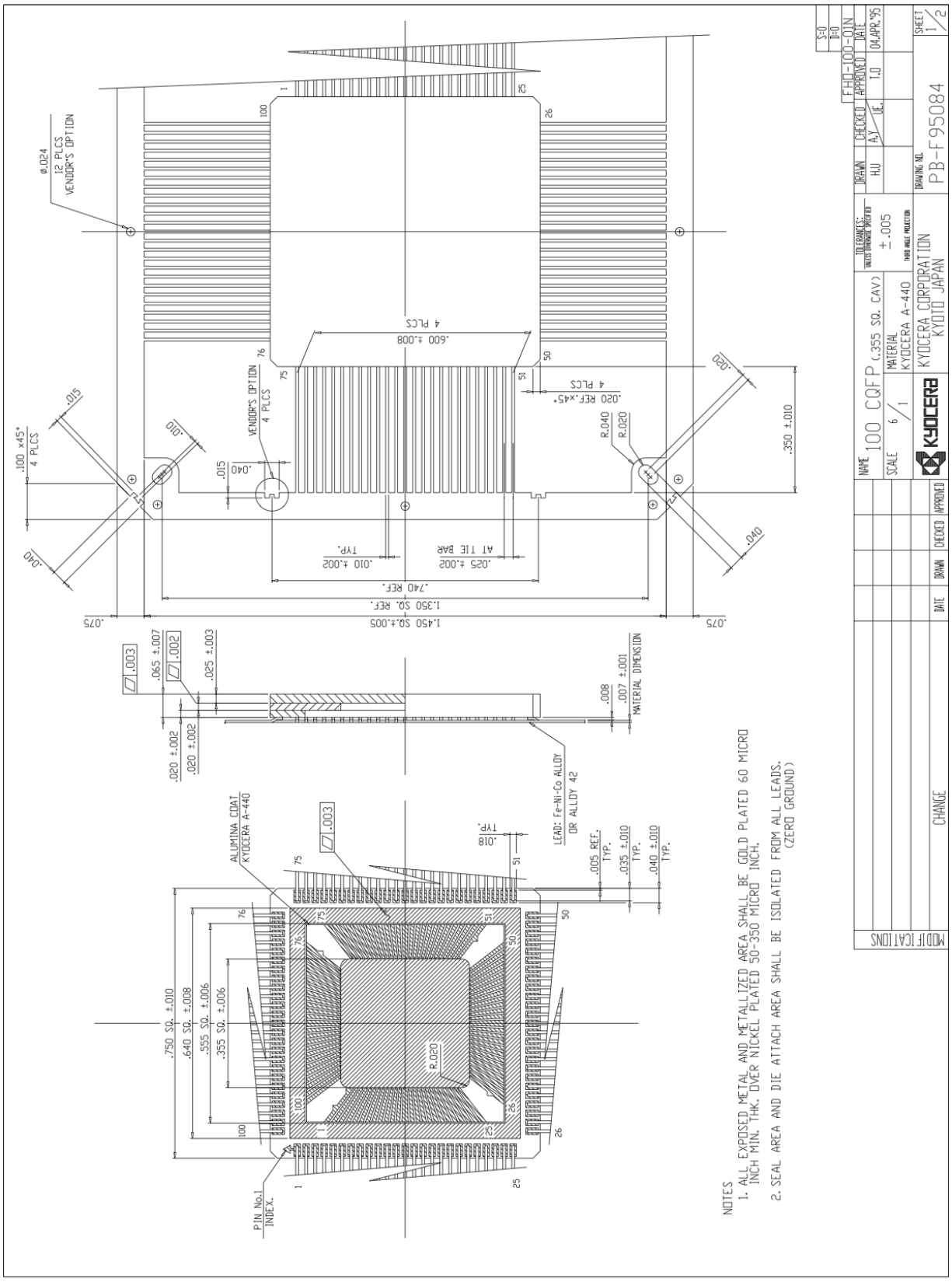

Figure 2: SIF2 (8 channel configuration) 100 pin package drawing.

2.2 Bare Die Dimensions

The size of the bare die is 4930 μm x 4930 μm.

2.3 Weight

The weight of the pSIF2 device (die and package) is TBD.

3 Electrical Parameters

The electrical parameters of the SIF2 device, as well as the typical and corner values are listed in table 6.

Table 6: Electrical characteristics of the pSIF2 device.

Parameter	Conditions	Min.	Typ.	Max.
2.5 V Power Supply (V)		2.25	2.5	2.75
3.3 V Power Supply (V)		2.97	3.3	3.63
2.5 V Power Supply Current (mA)			3	8
3.3 V Power Supply Current (mA)			0.5	1
High level Input Voltage V_{IH} (V)		2		
Low level Input Voltage V_{IL} (V)				0.8
Low level Output Voltage V_{OL} (V)	I_{OUT}=1mA			0.31
High level Output Voltage V_{OH} (V)	I_{OUT}=1mA	3.1		
Input Pad Capacitance C_{IN}(pF)		3	5	6
IO Pad Capacitance C_{IO}(pF)		4	6	7
Low Level Input Current I_{IL} (mA)				0.01
High Level Input Current I_{IH} (mA)				0.01
2.5 V Stand by Current $I_{STDBY2p5}$ (mA)		3	4	
3.3 V Stand by Current $I_{STDBY3p3}$ (mA)			0.2	0.3
PT Biasing				
Bias Current (mA)		0.5	1	2
Temperature Variation (nA@1mA output and 5.2 V)			6	14
Maximum Output Voltage (V)			5.2	5.4
PSRR (dB - to 100 KHz)(dB)			84	90
Analog Input Signal				
Differential Gain	Selectable	10		100
Gain Mismatch	Selected Gain = 100			0.1dB
BW(KHz)			100	
Input Common Mode (V)		1	2.7	
PSRR (dB - to 100 KHz)(dB)			84	90
ADC				
Offset (LSB)			0.5	1
DNL (LSB)			0.2	0.5
INL (LSB)			0.5	4
Sampling Rate (KSPS)			100	200
Temperature Measurement				
I_{BIAS} (mA)		1	1	3
$V_{OUT,MAX}$ (V)		2.4	2.45	2.6
Temperature Variation (nA@1mA output)			5	10
PSRR (dB - to 100 KHz)		84	90	
Voltage Reference				
TC (ppm/°C)			12	20
PSRR (dB - to 100 KHz)		84	90	
POR Characteristics				
POR Duration (msec)		50		
Digital Timings				
Compliance with HS I2C Standard			yes	
SPI			yes	

4 Digital Interfaces

4.1 I2C Interface

The digital I2C interface of the SIF2 ASIC allows:

- reading the device's ADC and configuration data as shown in Fig. 3
- writing configuration data to the device's control logic as shown in Fig. 4.

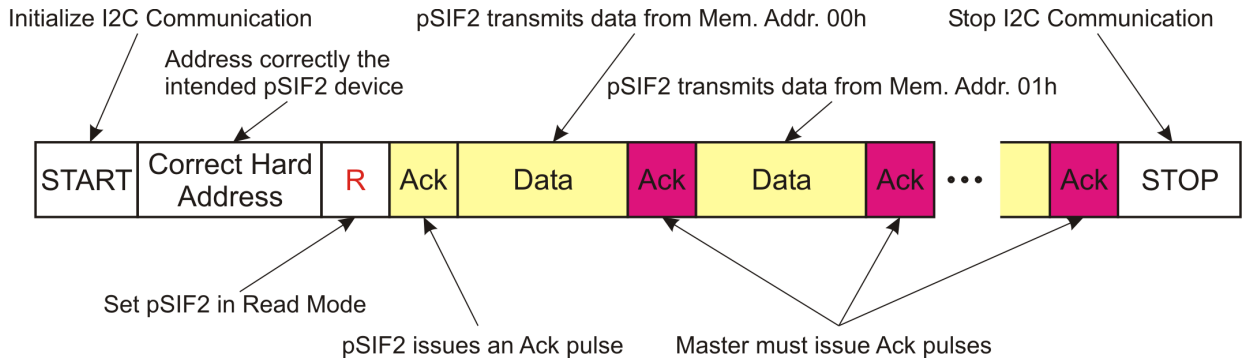

Figure 3: SIF2 Readout sequence though the ASIC's I2C interface.

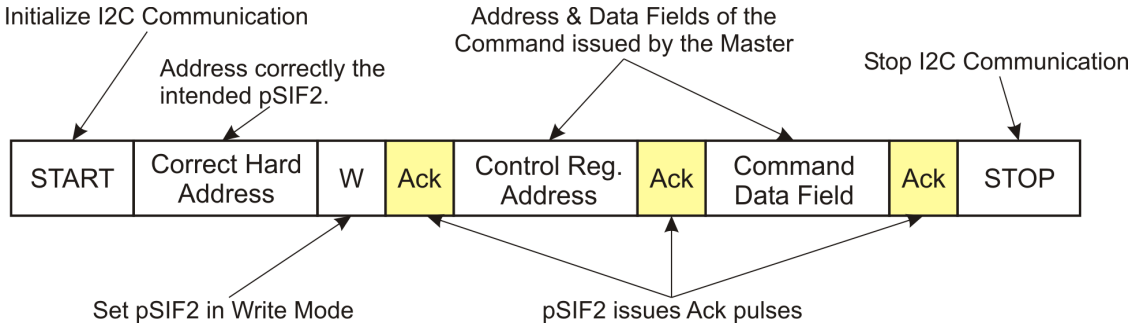

Figure 4: Sequence for issuing Commands to SIF2 through the I2C interface.

The timing diagram and the definitions/specifications of the involved signals are depicted in Fig. 5 and Fig. 6, respectively.

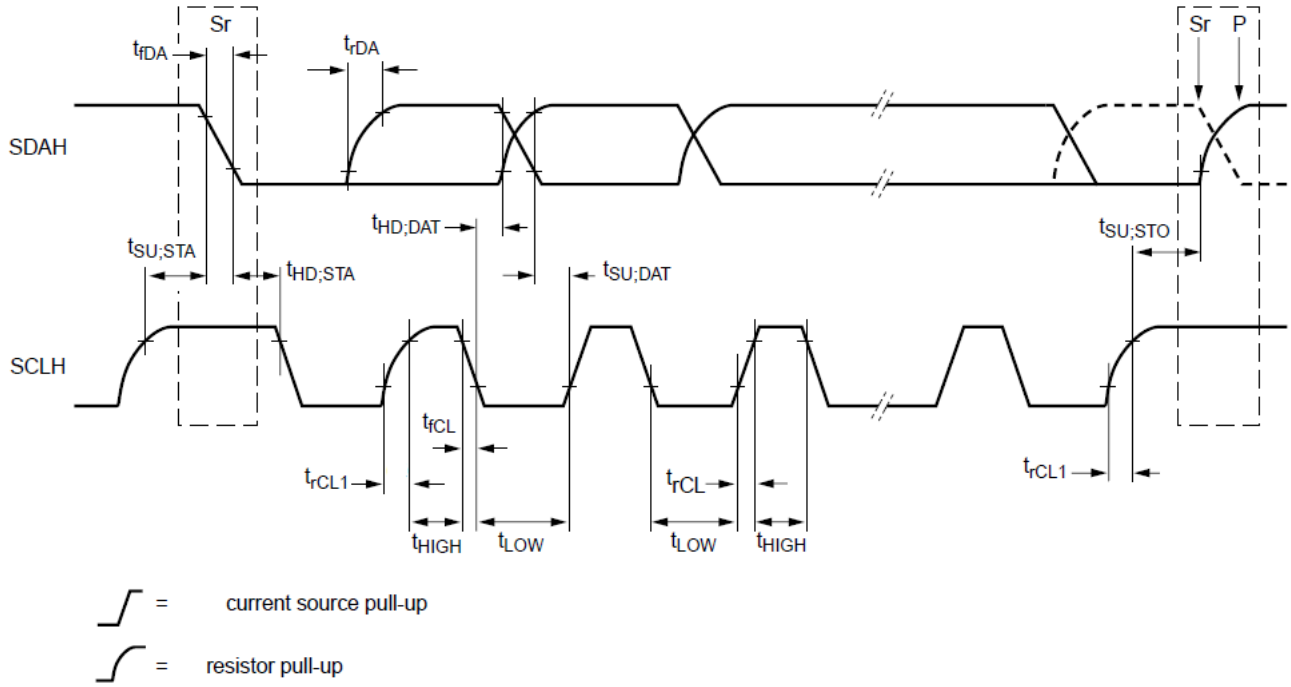

Figure 5: I2C interface communication (R/W) timing diagram.

Symbol	Parameter	Min	Max	Units
f_{SCLH}	Clock frequency	N/A	3.4	MHz
$t_{HD;STA}$	Hold time after start condition	160	N/A	ns
t_{LOW}	SCLH low duration	160	N/A	ns
t_{HIGH}	SCLH high duration	60	N/A	ns
$t_{SU;STA}$	Setup time for a repeated start condition	160	N/A	ns
$t_{HD;DAT}$	Data hold time	0	70	ns
$t_{SU;DAT}$	Data set-up time	10	N/A	ns
t_{BUF}	Bus free time between a stop and start condition	N/A	100	ns
$t_{VD;DAT}$	Data valid time	N/A	40	ns
t_{rCL}	Rise time of SCLH	10	40	ns
t_{rCL1}	Rise time of SCLH after a start or an Acknowledge	10	80	ns
t_{fCL}	Fall time of SCLH	10	40	ns
t_{rDA}	Rise time of SDAH	10	80	ns
t_{fDA}	Fall time of SDAH	10	80	ns
$t_{SU;STO}$	Setup time for stop condition	160	N/A	ns

Figure 6: I2C interface signals timing parameters definitions/specifications.

4.2 SPI Interface

The digital SPI interface of the SIF2 ASIC allows:

- reading the device's ADC and configuration data as shown in Fig. 7
- writing configuration data to the device's control logic as shown in Fig. 8.

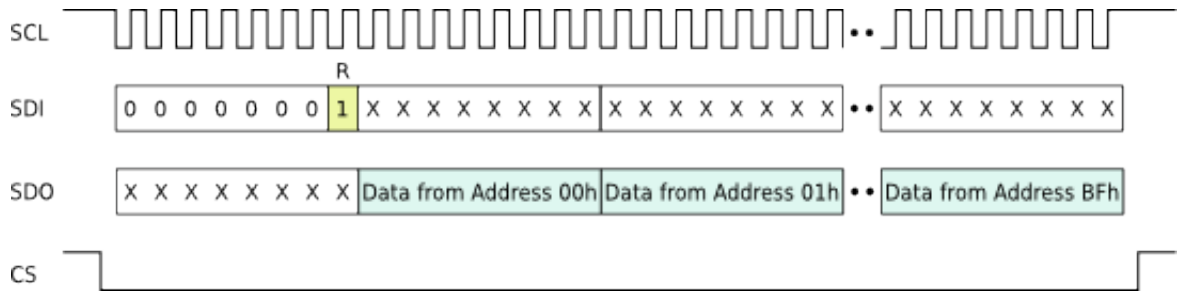

Figure 7: SIF2 Readout sequence though the ASIC's SPI interface.

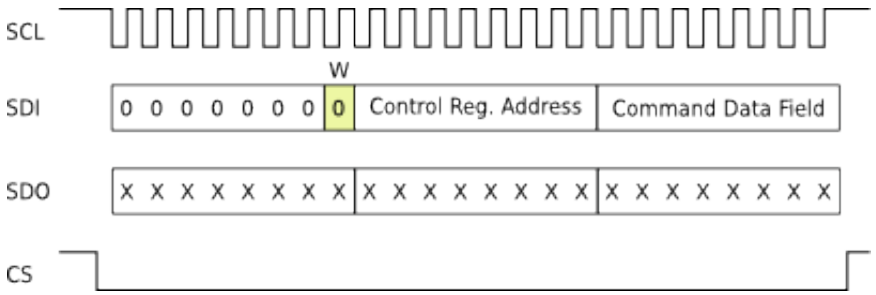

Figure 8: Sequence for issuing Commands to SIF2 through the SPI interface.

The timing diagram and the definitions/specifications of the involved signals are depicted in Fig. 9 and Fig. 10, respectively.

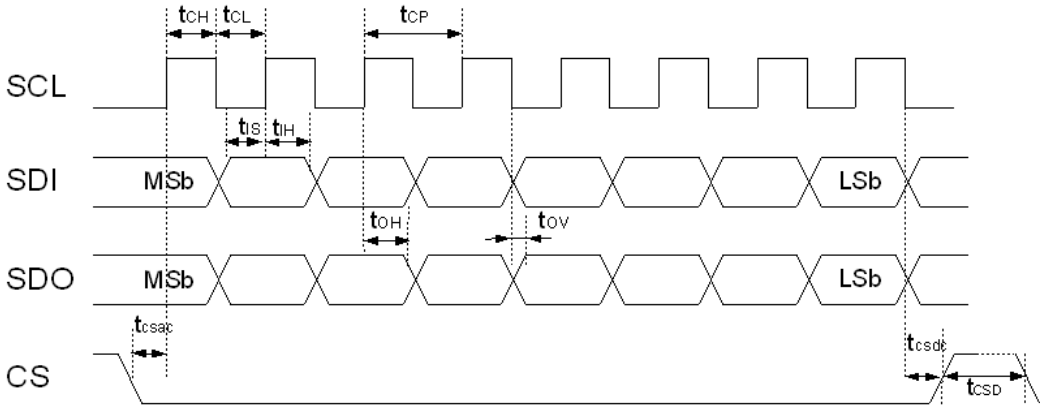

Figure 9: SPI interface communication (R/W) timing diagram.

Symbol	Parameter	Min	Max	Units
t_{CP}	Clock Period duration	40	N/A	ns
t_{CH}	Clock high duration	20	N/A	ns
t_{CL}	Clock low duration	20	N/A	ns
t_{IH}	SDI hold time	0,25	1	t_{CH}
t_{OV}	SDO data valid after clock time	N/A	5	ns
t_{IS}	SDI setup time	6	N/A	ns
t_{OH}	SDO hold time	18	N/A	ns
t_{CSAC}	Chip Select assertion to first rising clock edge	14	N/A	ns
t_{CSDC}	Last falling clock edge to Chip Select de-assertion	12	N/A	ns
t_{CSD}	Chip select de-assertion duration	16	N/A	ns

Figure 10: SPI interface signals timing parameters definitions/specifications.

5 Block Diagram

The block diagram of the SIF2 ASIC is shown in Fig. 11.

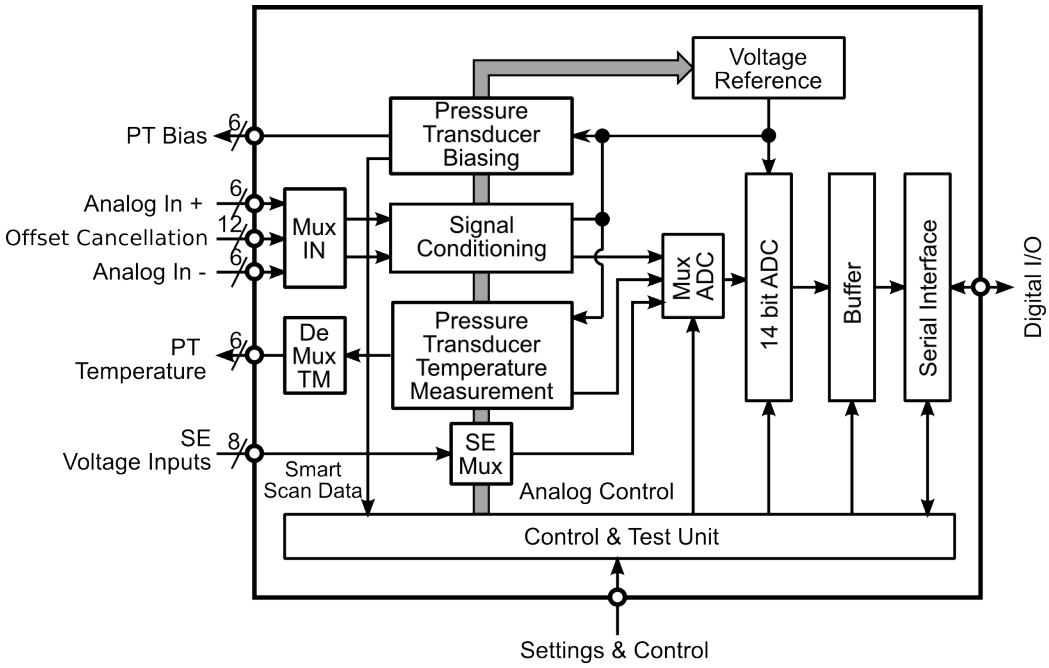

Figure 11: Block diagram of the SIF2 device.

6 Terminal Connections

The terminal connections is shown in table 7.

6.1 48 pin Configuration

Table 7: Terminal connections of the SIF2 ASIC

Lead	Pad Name	Lead	Pad Name	Lead	Pad Name	Lead	Pad Name
43	APID0	7	Bias	19	An_Test3	31	Int_Ext_Ref
44	HVVdd	8	Sel_IF_0	20	An_Test4	32	Abus_En
45	HGND	9	Sel_IF_1	21	DVdd	33	AVdd
46	APID1	10	$R_{C,T}$	22	VddIO	34	AGND
47	APID2	11	Vref,out	23	DGND	35	Vin(+)
48	APID3	12	Vref_1	24	MClk	36	Vin(-)
1	APID4	13	Vref_2	25	SDA	37	Voff(+)
2	APID5	14	Vref_3	26	SCL/TCK	38	Voff(-)
3	APID6	15	Ext_Ref	27	SDI/TDI	39	Bias_Sensor
4	iVR_Set	16	HVVdd	28	SDO/TDO	40	Rc_Sensor
5	HVVdd	17	An_Test1	29	CS/TMS	41	Temp_Sensor
6	HVGND	18	An_Test2	30	S_MClk_IEb	42	MReset

6.2 100 pin Configuration

Table 8: Terminal connections of the 100-pin CQFP packaged SIF2 ASIC (8 CH Configuration).

Lead	Pad Name	Lead	Pad Name	Lead	Pad Name	Lead	Pad Name
1	Vin(+)_2	26	Vin(+)_5	51	NC	76	NC
2	Vin(-)_2	27	Vin(-)_5	52	An_Test3	77	SE_Ch_En
3	Voff(+)_2	28	Voff(+)_5	53	An_Test4	78	NC
4	Voff(-)_2	29	Voff(-)_5	54	Int_Ext_Ref	79	Sel_IF_0
5	HVVdd	30	Bias	55	iVR_Set	80	Sel_IF_1
6	HVGND	31	Bias_Sensor_5	56	NC	81	Abus_En
7	Bias_Sensor_2	32	Rc_Sensor_5	57	APID0	82	AVdd
8	Rc_Sensor_2	33	Temp_Sensor_5	58	APID1	83	AGND
9	Temp_Sensor_2	34	$R_{C,T}$	59	APID2	84	Vin(+)_0
10	Vin(+)_3	35	Vref_out	60	DVdd	85	Vin(-)_0
11	Vin(-)_3	36	Vref_1	61	VddIO	86	Voff(+)_0
12	Voff(+)_3	37	Vref_2	62	DGND	87	Voff(-)_0
13	Voff(-)_3	38	Vref_3	63	MCLK	88	Bias_Sensor_0
14	Bias_Sensor_3	39	Ext_Ref	64	APID3	89	Rc_Sensor_0
15	Rc_Sensor_3	40	HVVdd	65	APID4	90	Temp_Sensor_0
16	Temp_Sensor_3	41	Vin_SE_Ch0	66	APID5	91	Vin(+)_1
17	Vin(+)_4	42	Vin_SE_Ch1	67	APID6	92	Vin(-)_1
18	Vin(-)_4	43	Vin_SE_Ch2	68	SDA	93	Voff(+)_1
19	Voff(+)_4	44	Vin_SE_Ch3	69	SCL/TCK	94	Voff(-)_1
20	Voff(-)_4	45	Vin_SE_Ch4	70	SDI/TDI	95	Bias_Sensor_1
21	HVVdd	46	Vin_SE_Ch5	71	SDO/TDO	96	Rc_Sensor_1
22	HVGND	47	Vin_SE_Ch6	72	CS/TMS	97	Temp_Sensor_1
23	Bias_Sensor_4	48	Vin_SE_Ch7	73	S_MClk_IEb	98	NC
24	Rc_Sensor_4	49	AnTest_1	74	1PT_6CH_Conf	99	MReset
25	Temp_Sensor_4	50	AnTest_2	75	NC	100	NC

7 Screening, Burn-in and Acceptance Requirements

7.1 SAF and IDDQ

SAF and IDDQ tests shall be performed in the screening board. **For the test procedure to be considered successful, all steps of the SAF and IDDQ procedures should be a pass.**

7.1.1 Burn-in Tests

All devices shall have passed the burn-in test (according to Test Method 1015 of MIL-STD-883). The parameters to be measured upon completion of the tests are listed in table 6. The measurements shall be performed at T_{amb} = 22°C $\pm$ 3°C. The maximum allowable drift values for the parameters that are allowed to change after burn-in are listed in table 9.

7.2 Allowable Drifts

Table 9: Allowable Drift Values after burn-in test.

Parameter	Conditions	Test Method	Drift
2.5 V Power Supply Current (μA)			$\pm$ 10
3.3 V Power Supply Current (μA)			$\pm$ 10
5 V Power Supply Current (μA)			$\pm$ 10
High level Input Voltage V_{IH} (mV)			$\pm$100
Low level Input Voltage V_{IL} (mV)			$\pm$100
Low level Output Voltage V_{OL} (mV)			$\pm$100
High level Output Voltage V_{OH} (mV)			$\pm$100
Low Level Input Current I_{IL} (μA)			0.2
High Level Input Current I_{IH} (μA)			0.2
2.5 V Stand by Current $I_{STDBY2p5}$ (μA)			1
3.3 V Stand by Current $I_{STDBY3p3}$ (μA)			1
5 V Stand by Current $I_{STDBY3p3}$ (μA)			5
PT Biasing			
Bias Current (nA)			5
Temperature Variation (nA@1mA output and 5/2V)			5
Maximum Output Voltage (mV)			10
PSRR (dB - to 100 KHz)(dB)			2
Analog Input Signal			
Differential Gain	Selectable		0.001
Gain Mismatch	Selected Gain = 100		0.1dB
BW(KHz)			0.1
Input Common Mode (mV)			5
PSRR (dB - to 100 KHz)(dB)			2
ADC			
Offset (LSB)			0.5
DNL (LSB)			0.1
INL (LSB)			0.3
Sampling Rate (KSPS)			0.1
Temperature Measurement			
I_{BIAS} (nA)			5
$V_{OUT,MAX}$ (mV)			10
Temperature Variation (nA@1mA output)			5
PSRR (dB - to 100 KHz)			1
Voltage Reference			
TC (ppm/°C)			2
PSRR (dB - to 100 KHz)			2
POR Characteristics			
POR Duration (msec)			0.5

Continued on next page

– continued from previous page			
Parameter	Conditions	Test Method	Drift
Digital Timings			
Compliance with HS I2C Standard			yes
SPI			yes

7.3 Functional Tests

The functional tests shall be performed at the following temperatures and power supplies:

Temperature	-55	25	125	(°C)
Power Supply	2.97	3.3	3.63	(V)

The absolute values, as well as the maximum allowable parameter deviations due to temperature and power supply variations, are listed in tables 6 and 9, respectively.

7.4 Failed Devices

Devices that fail in one of the above tests (if workable) may be used as engineering de-rated models.

8 Lot Acceptance Tests

Lot acceptance tests shall be performed according to ESCC basic specification no 9000.

9 Marking

When SIF2 devices are shipped to SPACE ASICS from the Packaging House they will be marked with respect to:

- Lead identification
- Component number
- Traceability information
- Manufacturer information

Marking will be performed according to ESCC basic specification no. 21700.

9.1 Lead Identification

The pin one indication shall be placed on top of the package.

9.2 Component Number

Each device shall be marked with the component number as shown below

pSIF2DMxxxx

where,
DMxxxx represents the **die** manufacturing date code.

9.3 Traceability Information

Each device shall be marked with the following traceability information

MFxxxx**LC**xx
SNxxxx **Conf**

where,
LCxx represents the lot code.
MFxxxx represents the manufacturing (assembly) date code.
SNxxxx is the serial number of the device.
Conf represents the packaging configuration of the device (S for single PT, A, for 8 channel ADC and M for 6 channel PT and 8 channel ADC).

9.4 Manufacturer Information

Each device shall be marked with the following manufacturer information

SPACE-ASICS

9.5 Example

An example is shown in Fig. 12.

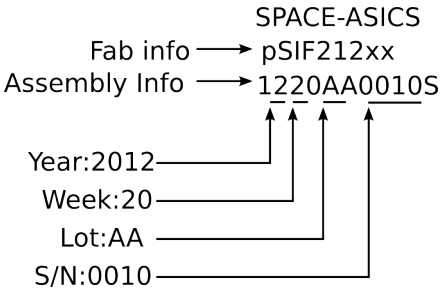

Figure 12: Example showing the component number, traceability and manufacturer information on the SIF2 ASICs.

10 Protective Packaging

SIF2 ASICs shall be delivered in ESD protective plastic boxes. Each box shall be able to contain 2 SIF2 devices (max). An ESD compliant sticker will be on the box stating the serial numbers of the SIF2 devices included.

11 Storage

The storage requirements of the device are listed in table 10.

Table 10: Storage requirements for the SIF2 device.

Temperature (°C)	**Min**	**Max**
	-55	160
Humidity (%)	**Min**	**Max**
	TBD	TBD