DEMOCRITUS UNIVERSITY OF THRACE
SPACE RESEARCH LABORATORY

space Asics

EM-pSIF ASIC BROCHURE

Doc ID	:	D-SA-pSIF-Br
Version	:	1.B
Date	:	March 30, 2010
Classification	:	For public release

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Introduction

The pressure sensor interface ASIC (pSIF) is a device, developed by DUTH/SRL, to interface (both bias and quantize) space qualified pressure sensors. It can be also used with various strain gauge type of sensors (displacement measurement,etc) .

pSIF Main Functionalities

- Bias the sensor with either a constant voltage or a constant current.
- Quantize the differential sensor voltage and the sensor voltage Vs and Vr
- Transmit the quantized sensor data to the S/C through the I2C bus.
- Handle up to 4 sensors simultaneously

Key Features

- Programmable gain amplifier in the DSE
- 14 bit ADC (12 true)
- Power Consumption <15mW
- TID Hardness > 1Mrad
- No SELs up to $80 MeV/mg/cm^2$
- No SEUs up to $80 MeV/mg/cm^2$

The block diagram of the pSIF device is shown in Fig. 1.

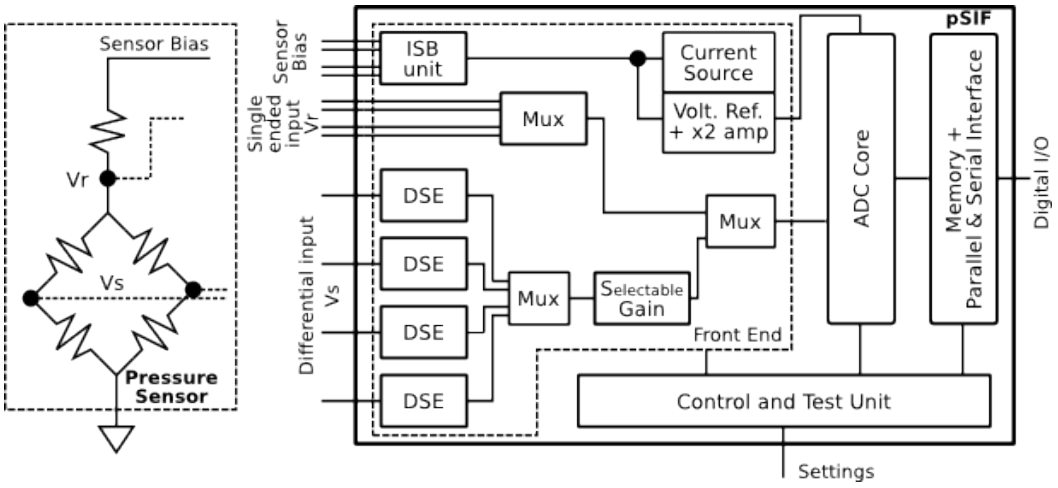

Figure 1: Block diagram of the EM pSIF device.

It consists of:

- ISB Circuit that handles the biasing of the sensors attached to the device

- 4 Differential to Single Ended (DSE) conversion units (one per sensor). The DSE stages apart from converting the differential voltage to a single ended, they also provide a gain of 20dB.
- A programmable amplification unit (pgain). The gain of this unit is programmed through an I2C/parallel command.
- 3 Multiplexers that direct the input voltages to the ADC core
- A Current Source that is used for providing a bias current to the sensor.
- A Voltage Reference unit which includes a bandgap reference and an x2 amplifier.
- A 14 bit ADC core
- A Memory together with a parallel and serial interface unit.
- A Control and Test Unit

1 Power Supply Characteristics

pSIF is fabricated on a 0.25um bulk CMOS process. The core unit requires a Vdd of 2.5V. Thick gate oxide transistors (that can be operated at 3.3V power supplies) are used for the I2C interface. Thus, pSIF has two independent power supply lines; one for the 3.3V and one for the 2.5V. In order for the device to be easy to use and attractive, an internal power supply regulator is implemented. The power supply regulator produces internally the 2.5V core Vdd from the 3.3V power supply line.

- The power supply regulator has the ability to be de-activated through an external pad. In this case the user has to provide both the 3.3 and 2.5V power supplies to the ASIC.
- In case the power supply regulator is activated the user can only supply the 3.3V Vdd to the device. The 2.5V are produced internally.
- In addition the user can deactivate the power supply regulator and provide on both power supply lines 2.5V. In this case the device functions properly with the exception that the I2C interface operates at 2.5V.

The block diagram of the internal voltage regulator is shown in Fig. 2.

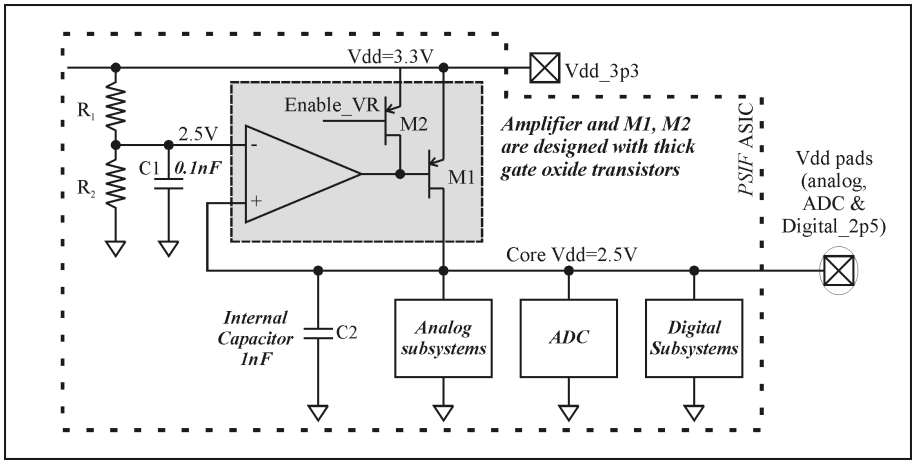

Figure 2: Block diagram of the internal voltage regulator.

2 Active Sensor Biasing

There are two ways to bias the sensor:

- Through a constant voltage.
- Through a constant current.

The selection between these two configurations is performed through a command. By default constant current biasing is selected. However, there are some external connections that need to be implemented so that the optimum performance is obtained.

2.1 Constant Voltage Biasing Setup

In this case an internal amplifier is used to provide a constant voltage to the sensors. The following pads are used:

- Vin_x2_amp (input to the amplifier)
- BG (Output of the bandgap reference). The use of this pad is optional.

The external configurations needed for the constant voltage biasing setup are shown in Fig. 3. The user must externally connect the output of the bandgap reference to the input of the amplifier (red line in Fig. 3). If the user wants to provide another voltage he must directly connect it to the input of the amplifier. In this case the output of the bandgap reference must not be connected to the input of the amplifier.

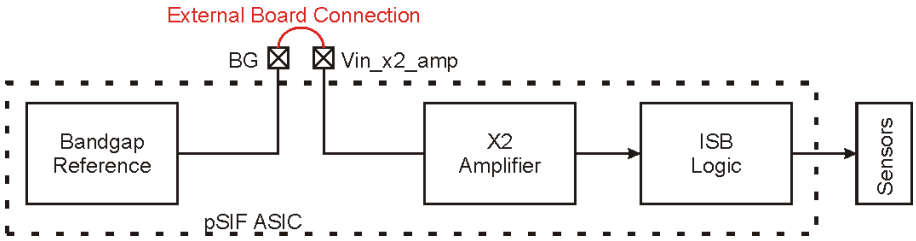

Figure 3: Constant voltage configuration setup.

2.2 Constant Current Biasing Setup

In this configuration the user needs to define the output current by means of an external resistor. The resistor needs to be external because it needs to have a small temperature coefficient. In the constant current biasing configuration the following pads are used.

- R_C
- CS_V+_R1

The external configurations needed for the constant current biasing setup are shown in Fig. 4. The user must connect a low temperature coefficient resistor (Rc) from pad Rc to pad CS_V+_R1. He must also connect pad CS_V+_R1 to a voltage source. Analog Vdd would be sufficient for the purpose of pSIF applications.

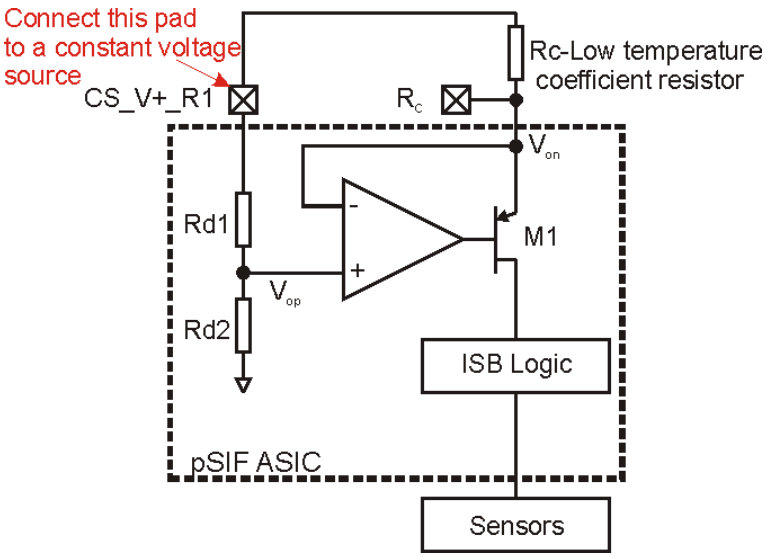

Figure 4: Constant current configuration setup.

3 Inactive Sensor Bias Configuration

pSIF can bias the pressure sensor either with a constant voltage or a constant current. The selection is performed through a command issued from the I2C bus. During the time that a specific sensor is interfaced, the other three sensors connected to the pSIF device (inactive sensors) are kept in a biased state through the inactive sensor bias (ISB) subsystem of the ASIC. The ISB circuit has the ability to be de-activated. The biasing of the inactive sensors is essential to guarantee a good performance. The sensor biasing network is shown in Fig. 5. A copy of the developed voltage (no matter if it is biased on constant voltage or constant current) on the active sensor is copied to the inactive ones through buffers B1-B4.

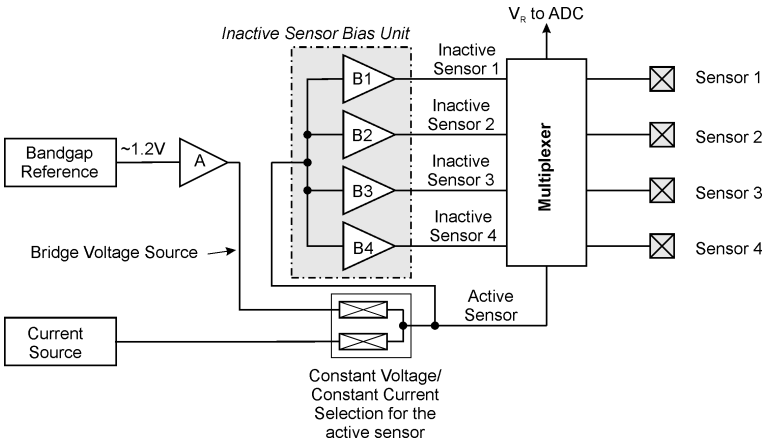

Figure 5: Block diagram of the sensor biasing unit of pSIF.

4 Sensor Interface Setup

The sensor-pSIF ASIC interface is shown in Fig. 6. Only one sensor (out of the 4 that can be attached) is shown for simplicity reasons. Pad BS is used to bias the sensor. Pad VR is the single ended voltage that is converted directly through the ADC and is used for temperature compensation of the sensor. Pads Vin+ and Vin- are connected directly to the sensor. It is through these pads that the differential bridge voltage is fed into the pSIF ASIC. Pads Voff+ and Voff- are used to add/subtract an offset voltage to the differential bridge voltage. The offset voltage is set through external resistors R1-R3 as shown in Fig. 7. The values of R1, R2 and R3 are defined per chip and per sensor.

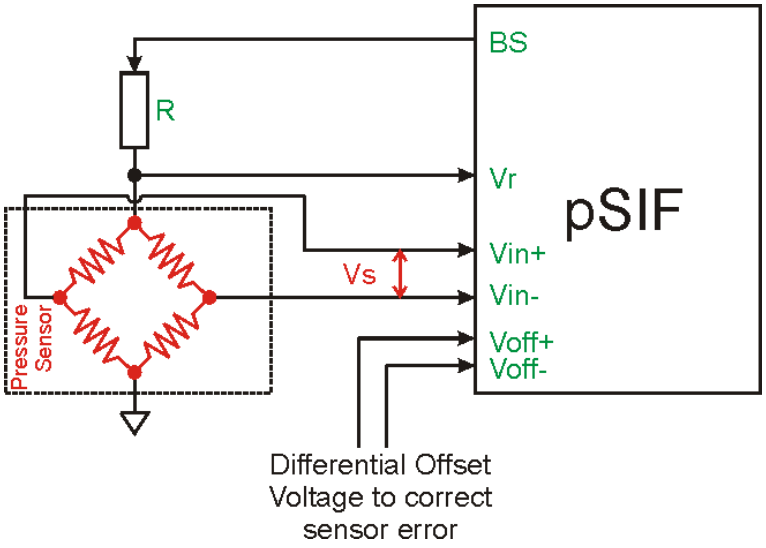

Figure 6: Block diagram for the EM pSIF sensor interface setup.

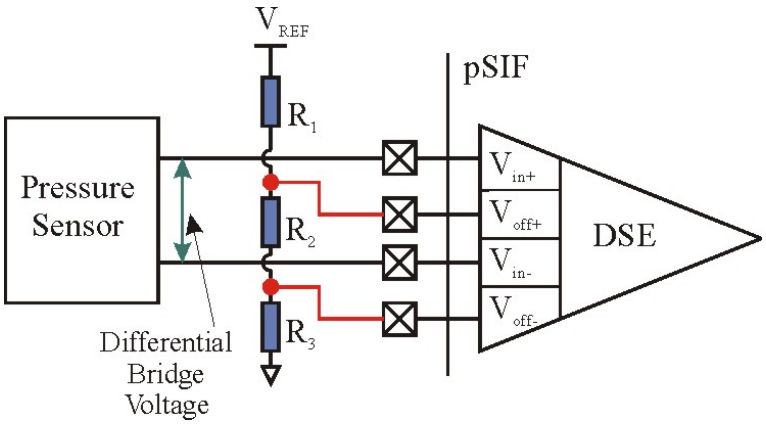

Figure 7: Generation of Voff+ and Voff-.

5 Gain Selection

4 gain values are provisioned in the pSIF device for the differential bridge voltage Vs: 100, 800, 6400, 10000. The user can select any of these configurations depending on the full scale pressure that needs to be measured and the pressure sensor used. The selection is done through the I2C interface.
Important Note: Bye connecting the sensor to Voff+ and Voff- and applying the offset correction voltages to Vin+ and Vin-, the gain values become 10, 80, 640, 1000

6 Fix-Scan Configuration

pSIF device has two modes of measurement regarding the 4 sensors that it interfaces. In the scan mode the device quantizes each sensor sequentially. In the fix mode it performs ADC conversions only on one sensor. The sensor that is interfaced is programmed by a command. The command can be issued by either the serial or the parallel interface.

7 Internal Register Map

There are two types of registers inside the pSIF ASIC.

- Memory registers
- Command registers

Both registers can be accessed through both the parallel and the serial interface.

7.1 Memory Registers

An internal memory is used so that sensor data can be stored until they are read by the user. Both VR and VS from each sensor will be stored into the memory. Each sensor data will be stored to a different memory location. Thus the capacity of the memory shall be 8x14 bits. Data shall be written into the memory only through the ADC and be read either through the parallel or the serial bus. The memory connectivity with the ADC and the parallel and serial bus is shown in Fig. 8. For each sensor two memory locations are allocated: one for the bridge excitation voltage (VR) and one for the differential bridge voltage (VS). Both voltages require 14 bits. To accommodate the four sensors interfaced by the ASIC, eight (8) memory locations are required. The block diagram of the memory is shown in Fig. 9. The memory map as seen from the parallel and from the serial port of the device is shown in Fig. 10. From a single parallel address a direct 14 bit word is read. For a complete read out of the sensor two memory locations must be addressed. From a single serial address only 8 out of 14 bits are accessed from the memory. For the whole word to be accessed two consecutive read outs must take place. In the first readout the 8 MSB bits from the 14-bit word are accessed and in the second the 8 LSBs (2 bits are common in both readouts). Thus, 4 serial addresses must be used for a complete read out of the sensor from the serial bus. For compatibility reasons the serial and parallel address required to access a memory location are identical as shown in Fig. 10.

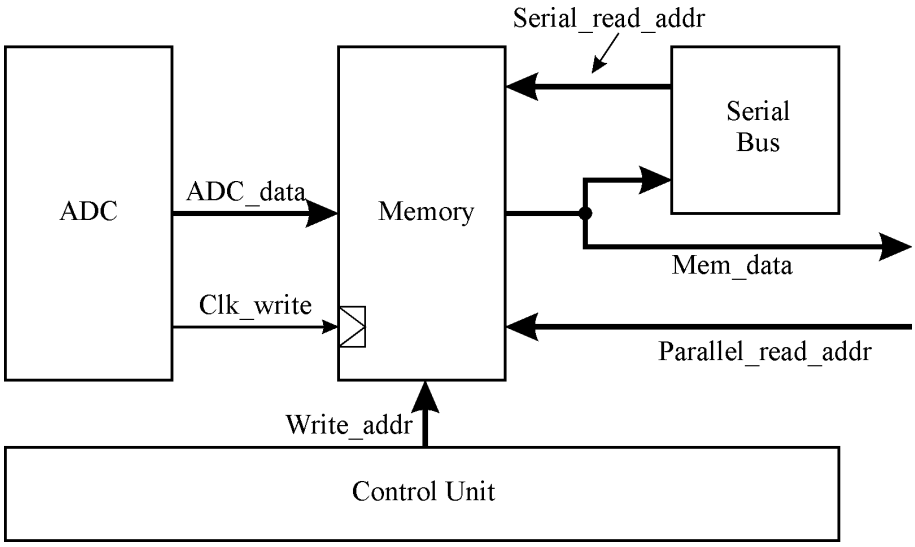

Figure 8: Block diagram showing the connectivity of the memory with the parallel and the serial bus.

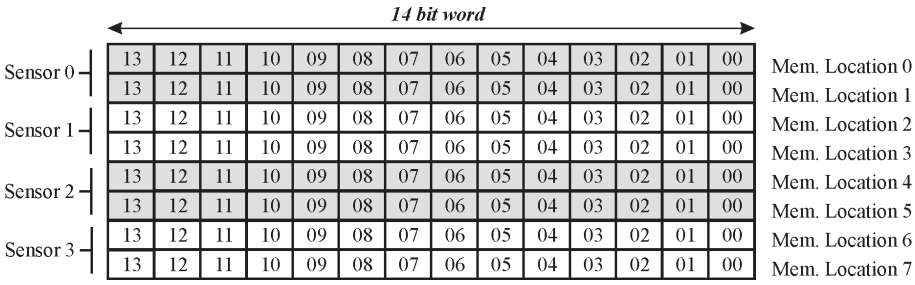

Figure 9: Block diagram of the pSIF memory.

7.2 Command Registers

The commands implemented in the pSIF ASIC are listed in the following table.

8 pSIF Interfaces

8.1 I2C Interface

The I2C unit, implemented in the pSIF ASIC, can operate only in slave mode. This means that there must be a master on the bus that will initiate the communication. The main tasks the internal I2C performs are:

- Receive commands via the I2C bus from the master

Sensor	*Parallel Address*	*Voltage returned*	*Serial Address*	*Voltage returned*
Sensor 0	H00	Vr	H00	Vr (8 MSB)
			H01	Vr (8 LSB)
	H02	Vs	H02	Vs (8 MSB)
			H03	Vs (8 LSB)
Sensor 1	H04	Vr	H04	Vr (8 MSB)
			H05	Vr (8 LSB)
	H06	Vs	H06	Vs (8 MSB)
			H07	Vs (8 LSB)
Sensor 2	H08	Vr	H08	Vr (8 MSB)
			H09	Vr (8 LSB)
	H0a	Vs	H0a	Vs (8 MSB)
			H0b	Vs (8 LSB)
Sensor 3	H0c	Vr	H0c	Vr (8 MSB)
			H0d	Vr (8 LSB)
	H0e	Vs	H0e	Vs (8 MSB)
			H0f	Vs (8 LSB)

Figure 10: Block diagram explaining how to address the memory from the parallel and the serial interface.

- Send data through the I2C bus to the master.

The data can either be ADC (which are read from the memory) or status data. In Fig. 11 the internal interfaces of the I2C are depicted. The internal interfaces are listed below:

- I2C Address (red line). This is the address bus that comes from the internal I2C interface and is used for addressing the various subsystems inside the pSIF. It is important to note that the user must not confuse the I2C Address bus (internal green line) with the 7 bit I2C_hard_address black thick line which is used to set the address of the specific I2C, i.e the address for which the specific pSIF will respond.
- I2C Data Out (blue line). Data/Commands that are sent from the master to pSIF are transferred internally from the I2C interface through this bus.
- I2C Data in (green line). Data that are requested by the master from the pSIF are transferred internally to the I2C interface through this bus.

The I2C bus housing one master and many pSIF devices is shown in Fig. 12. The bus consists of two lines:

Table 1: Commands implemented in the pSIF ASIC.

Command	Address	Data
Master Reset	h80	X
ADC Reset	h81	X
Memory Reset	h82	X
Fix Scan	h84	0 Scan 1 Fix
Constant Voltage/Current Bias	h85	0 Constant Current 1 Constant Voltage
ISB Unit	h86	0 Inactive 1 Active
Front End Gain	h88	0-3 100, 800, 6400 and 10000
Daz Setting	h8A	0 Daz Off 1 Daz On

- The serial data bus (SDA) line.
- The serial clock (SCL) line.

The SDA line can be controlled both by the master (external microcontroller) and by any pSIF device that is transmitting. The SCL line is controlled only by the master. Up to 128 pSIF devices can be connected to the bus. Each device will have a unique serial address set by hard pins on the board level. Both SCL and SDA lines can be operated anywhere between 2.5 and 3.3V. The pull up resistor from the SDA line can be in the range from 120 Ohms to 10K.

8.1.1 Reading Data through the I2C Interface

The readout sequence in its simplest form is depicted in Fig. 13. The master initiates the communication via the I2C bus by issuing a start pulse and it addresses the intended pSIF in Read mode. pSIF will respond to the correct addressing by issuing an ACK pulse. After that it will start transmitting data stored in a memory location that corresponds to the I2C Address H00. Then it will wait for an ACK pulse from the master on the next clock. If this pulse is not issued by the master it will cease the communication. If it is issued, it will continue by sending the data from address H01 and so on. At this point it is important to note that:

- I2C interface logic will continue to update the I2C Address value until it reaches Hff before returning to H00

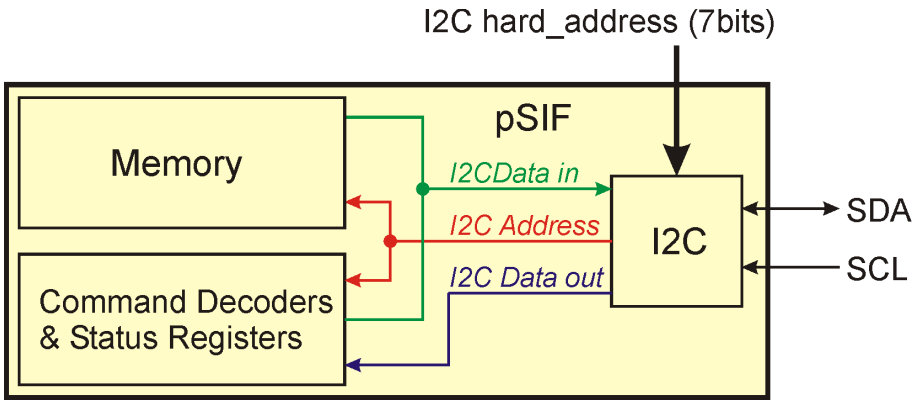

Figure 11: pSIF I2C unit's internal interfaces.

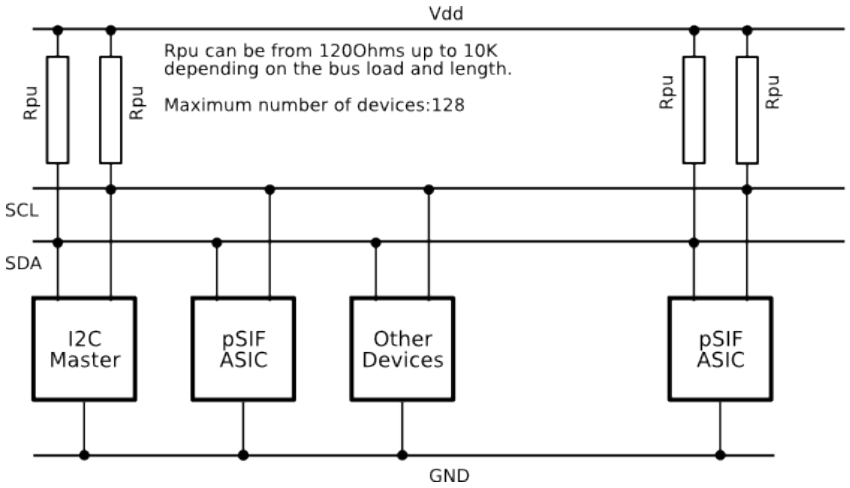

Figure 12: pSIF sitting on an I2C bus.

- After a stop command the I2C Address value is not reset.

As it will be shown later the useful addresses in the memory are from H00 up to H0f when 4 sensors are connected to the device and up to H03 when only one sensor is connected to the device. Thus, if the master wants to read just these values he needs to update the I2C Address value every time it has read the intended memory values. In order to update the I2C Address value the sequence depicted in Fig. 14 has to take place. The master addresses the intended pSIF, and sets it in write mode. After pSIF issues the ACK pulse, the master writes the I2C address value he wants (most probably H00). After this sequence the master can apply the sequence of Fig. 14.

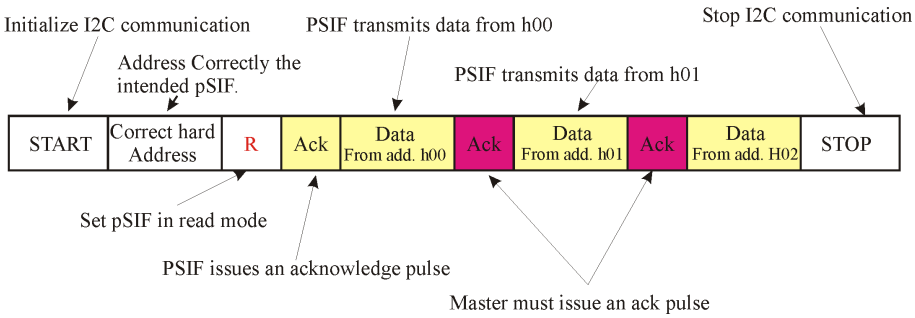

Figure 13: Simple Read out from the pSIF ASIC.

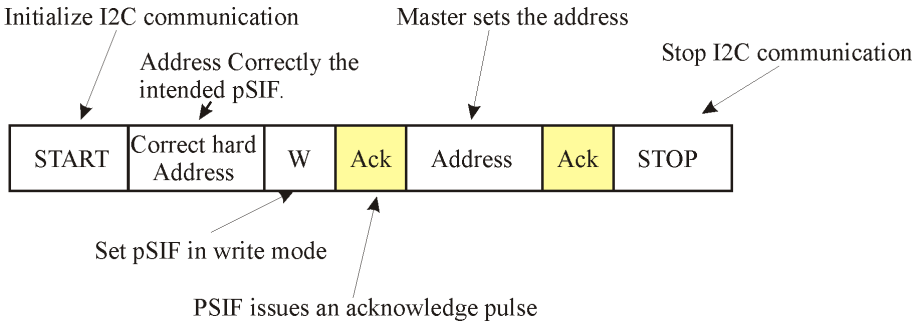

Figure 14: Setting the I2C Pointer.

8.1.2 Writing Data through the I2C Interface

In this section a description on how to issue commands to the pSIF through the I2C is given. The basic form of a command is shown in Fig. 15. The user issues a start condition, addresses the intended pSIF, waits for the ACK pulse and then gives consequently the address and the data for the command.

8.2 The Parallel Interface

The parallel interface is mostly used for testing purposes. It is advised not to be used in nominal operation since a lot of noise is induced. The parallel interface consists of the following pads/buses:

- A data bus (DB[13..0]) (bi-direectional bus)
- An address bus (AB[7..0]) (input bus)
- Pad CSb_par. Used to select the current chip.
- Pad RWb_par Used to select between read and write mode.

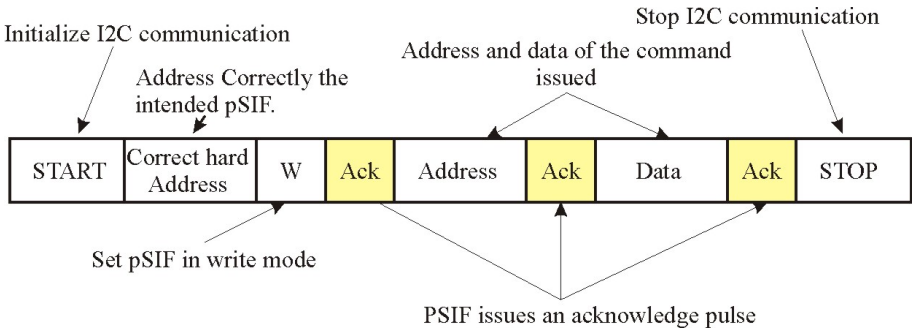

Figure 15: Command diagram for issuing commands to pSIF through the I2C interface.

When CSb_par is high the data bus is tri-stated. It is important to note that no internal pull up resistors exist. Thus the user needs to use external resistors to Vdd or GND.
The following characteristics apply when pSIF is written through the parallel bus. The worst case timings are shown in table 2. When reading through the parallel

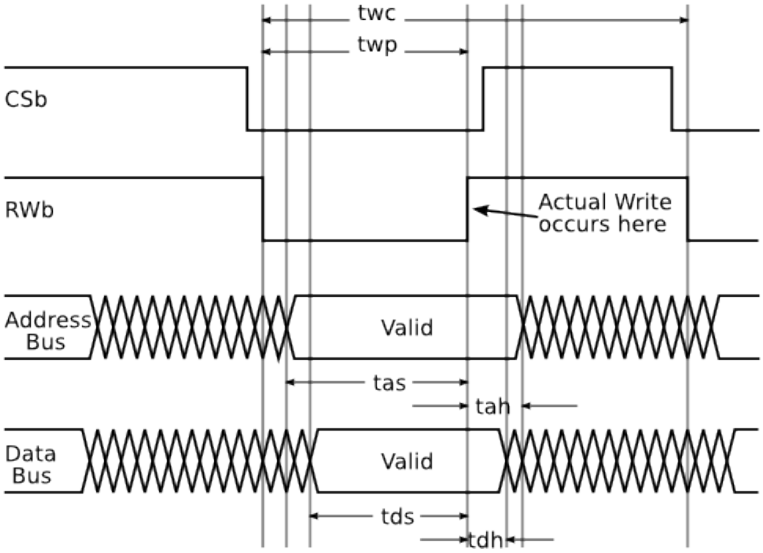

Figure 16: Timing diagram of the write function through the parallel interface.

bus, pad RWb is always kept high. The user drives the address bus and after 1.7 ns (worst case) the data are available on the bus.

Table 2: Parallel bus timing characteristics.

t_{WC}	Write Cycle	> 25ns
t_{WP}	Write Active Pulse	> 10ns
t_{AS}	Address Setup Time	> 6ns
t_{AH}	Address Hold Time	> 1ns
t_{DS}	Data Setup Time	> 5ns
t_{DH}	Data Hold Time	> 1ns

9 Analog Sampling Electrical Characteristics

The ADC characteristics are shown in the table 3. A typical INL of the ADC is shown in Fig. 17.

Table 3: Analog Sampling Characteristics

Full Scale Range	0-2.3V
INL on the ADC	±0.5LSB nominal, ±1 LSB after 1Mrad
Input Resistane	> 1GOhm
Input Capacitance	< 4pF
BW for Vs	300Hz typical Can be trimmed to any value between 100Hz-300KHz through bias resistor trimming.
BW for Vr	100KHz

The ADC has a digital AutoZeroing (DAZ) algorithm to correct TID induced offset in the comparator. The autozeroing option is selected through a command (either through the I2C or the parallel bus). When in AZ mode two conversions are made for every analog input so that the result is obtained. By doing so the offset of the comparator is cancelled out. DAZ is only used in cases where TID is expected to surpass 300Krad. In Fig. 18 the maximum INL versus TID with DAZ on is shown.

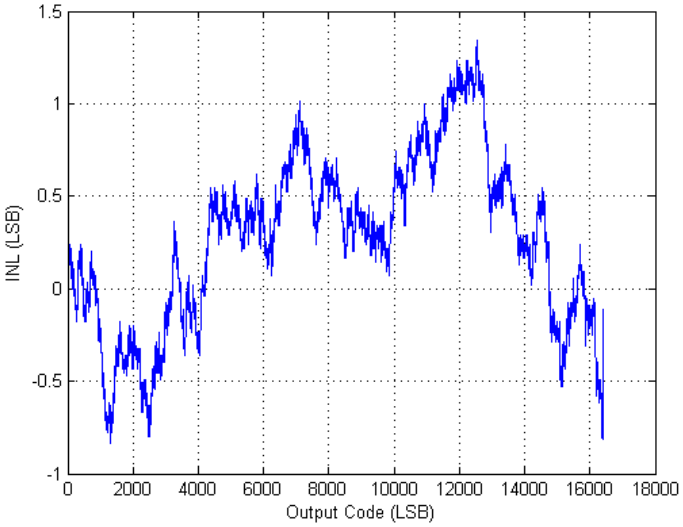

Figure 17: Typical INL curve for the ADC.

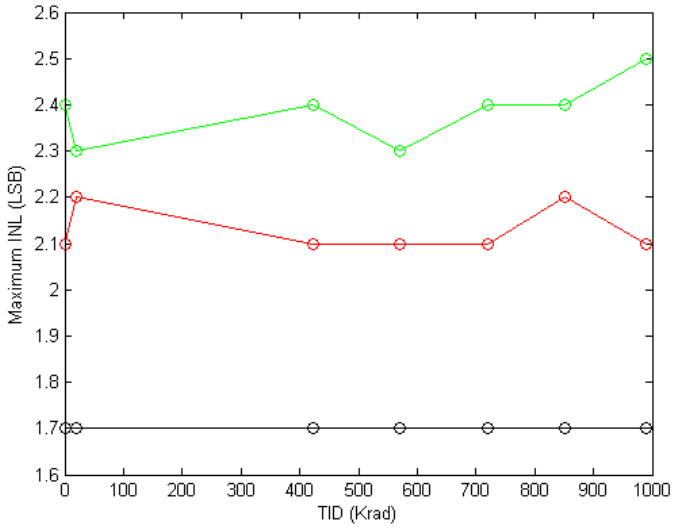

Figure 18: Maximum INL versus TID for three irradiated devices.

10 Power Supply Ratings

As discussed above, pSIF can be powered in three modes:
Single Power supply of 3.3V, dual power supply of 3.3 and 2.5V and single power supply of 2.5V.
In the first case the power supply can vary from 2.7V up to 3.7V. In the second case the 3.3V power supply can vary from 2.7 up to 3.3V and the 2.5V power supply can vary from 2 up to 2.8V. In the third case the power supply can vary from 2 up to 2.8V.

11 Temperature Characteristics

pSIF device can operate without performance degradation from -55 to 125 deg C. The maximum INL deviation versus temperature is shown in table 4.

Table 4: Temperature dependence of the ADC INL

Temperature	Maximum deviation from INL @ room temperature
-55	-0.25LSB
32	0.125LSB
41	0.25LSB
65	0.375LSB
73	0.375LSB
118	0.875LSB
153	1.875LSB

The performance of the bandgap reference vs temperature is shown in Fig. 19. An 1.5mV variation over the entire operating range of -55 to 125 degC is achieved.
The temperature characteristics of the x2 amplifier is shown in Fig. 20. The DC gain is not dependent on temperature variations. While this amplifier is used for DC signal amplification, it has a bandwidth of a few tens of KHz and temperature variation does not affect its performance.
The bode diagram of the DSE stage for the entire temperature operating range is shown in Fig. 21. As it can be seen the DC gain of the DSE stage is not affected at all by temperature. The -3dB frequency is affected (<50Hz) @ 300Hz, which is well beyond the BW characteristics of pSIF.

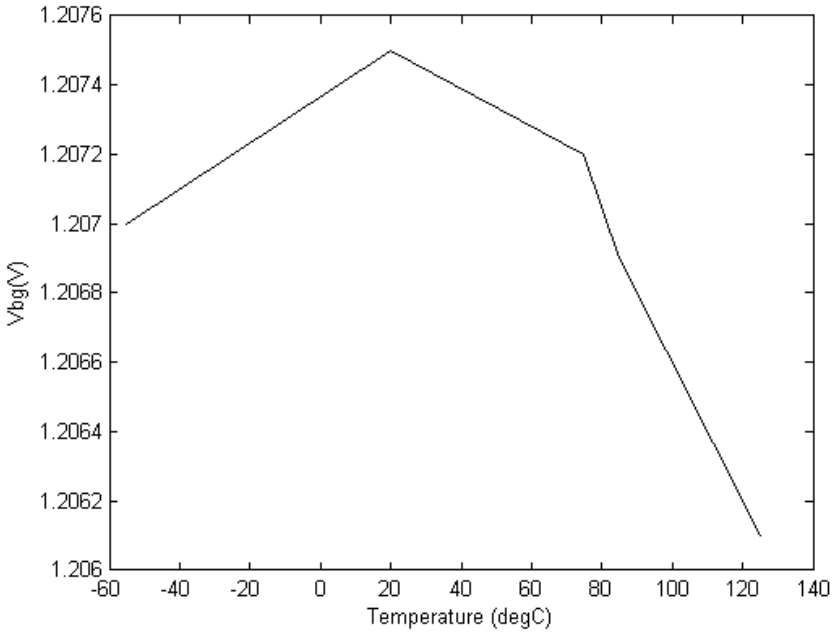

Figure 19: Bandgap reference performance vs temperature.

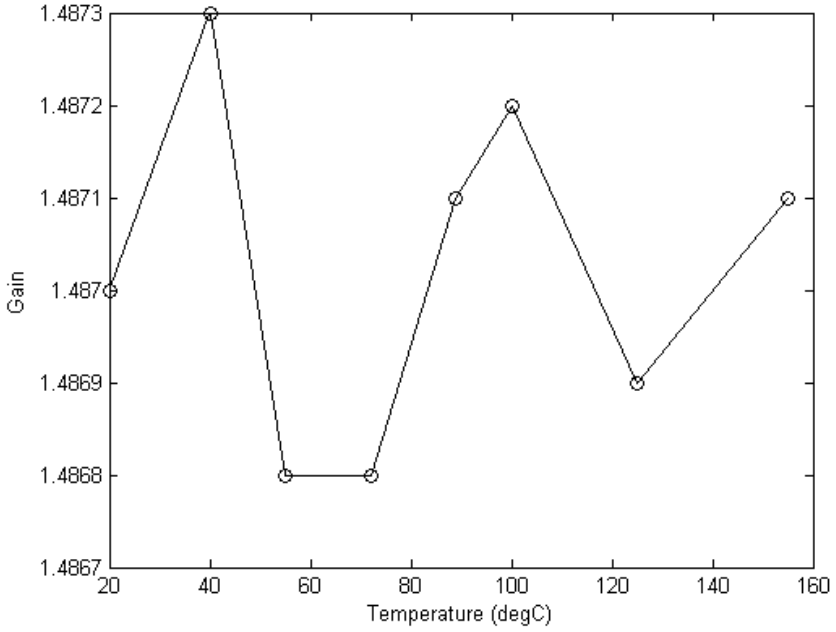

Figure 20: x2 amplifier performance vs temperature.

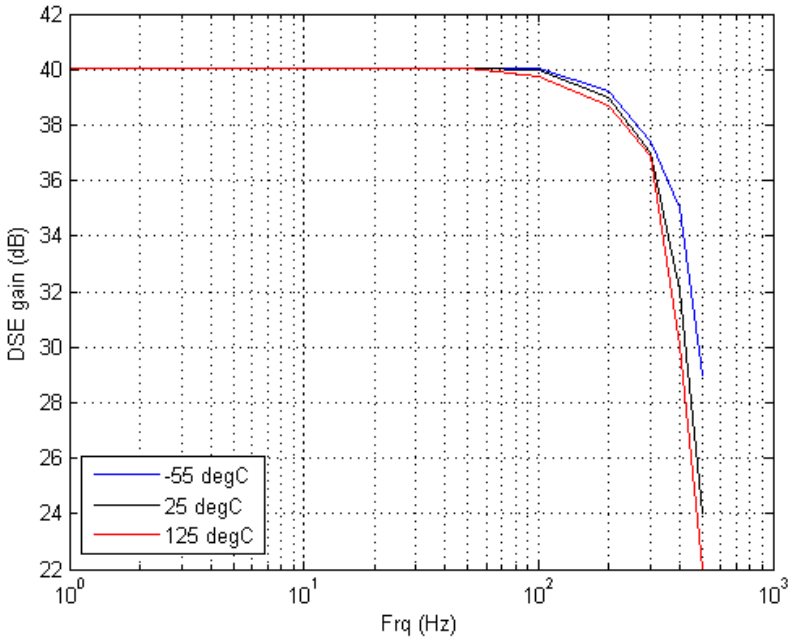

Figure 21: DSE performance vs temperature.

12 Power Consumption

The power consumption of the pSIF device is less than 25mW (worst case-4 sensors attached to the device) including the sensor current. For a single sensor the power consumption can be as low as 10mW.

13 Operating Frequency

pSIF contains an internal oscillator trimmed for 50Hz sampling on all of the 4 sensors. An ability to disable the internal oscillator and use instead an external oscillator is provided. The maximum input frequency in this case must be 20MHz. The sampling rate on the sensors in this case would be 200KHz.
At this point it should be noted that the EM version of pSIF does not contain a Sample and Hold circuit. Thus the input signal bandwidth must be contained below 200Hz so that resolution is not compromised. The DUTH/SRL and SPACE-ASICS team is currently designing a new version of the pSIF device, where a sample and hold circuit is included in the ADC enabling a sampling frequency of 200KHz

14 Radiation Hardness

14.1 Total Ionizing Dose

pSIF is rad-hard up to above 1 Mrad (Si). The leakage increase in the digital section is less than 1uA after 1Mrad.

14.2 Single Event Effects

Single event effects testing was performed on the device in the RADEF facility. No SEL occurred up to an LET value of 80 $MeV/mg/cm^2$. It should be noted that this was the highest LET that the device was tested at RADEF. The SEU threshold is at 80 $MeV/mg/cm^2$.

15 Packaging Information

pSIF is available as:

- 120 CQFP Package/Metal lid/
- Bare die

16 Other Applications

16.1 Temperature Measurements with pSIF

pSIF can be used for temperature measurement applications with positive temperature coefficient (PTC) or negative temperature coefficient (NTC) sensors according to ECSS-E-50-14 document. In order to perform temperature measurements the current source is utilized along with a low temperature coefficient external resistor so as to produce a nearly temperature independent current. The output current is fed to the sensor and the developed voltage is quantized by the ADC. The setup is shown in Fig. 22.

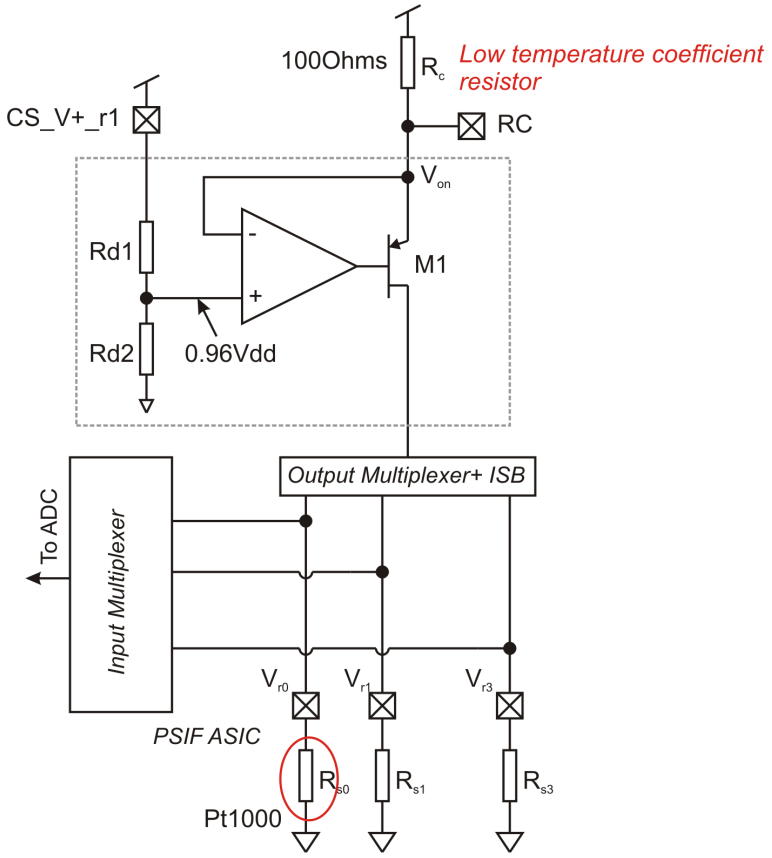

Figure 22: Setup for using the pSIF for temperature measurements utilizing the current source and an external low temperature coefficient resistor.

The output current of the current source is defined as

$$I_{OUT,CS} = \frac{0.04 \cdot Vdd}{R_C} \tag{1}$$

The voltage developed on a temperature sensor will be equal to

$$V_{SENSOR} = I_{OUT,CS} \cdot R_{SENSOR} = \frac{0.04 \cdot Vdd}{R_C} \cdot R_{SENSOR} \tag{2}$$

Assuming a PTC (PT1000) (information from ECSS-E-50-14) temperature sensor the voltage developed on the sensor will be equal to

$$V_{SENSOR} = \frac{0.04 \cdot Vdd}{R_C} \cdot R_{SENSOR\_TNOM} \cdot (1 + TC_{Rs} \cdot \Delta\Theta) \tag{3}$$

where, R_SENSOR_TNOM is the value of the sensor at 0 deg C temperature, TC_RS is the temperature coefficient of the PT1000 temperature sensor and

$\Delta\Theta$ is the sensor's temperature difference from reference temperature (zero degC).

The developed voltage is quantized by the ADC. At this point is should be noted that the ADC uses a Vdd reference so as to have a power supply ratio-metric measurement. Assuming an ideal ADC the output code will be equal to

$$OC = \frac{V_{Sensor}}{Vdd} = \frac{R_{SENSOR\_TNOM} \cdot (1 + TC_{Rs} \cdot \Delta\Theta)}{R_C} \cdot 0.04 \cdot 2^N \tag{4}$$

where, N is 14 (number of bits of the ADC). From eq.4 it can be seen that the output code of the ADC is dependent only on the temperature of the sensor and not on the power supply level. The user can then solve for $\Delta\Theta$ and find the temperature on the sensor.

16.1.1 Selecting the Components

In this section an analysis is presented on how to trim the performance of pSIF for temperature mode measurements. Assuming that a PT1000 (1K @ zero deg C) temperature sensor is used, the output code at room temperature would be equal to

$$OC_{ROOM} = 0.04 \cdot 2^N \tag{5}$$

The resolution in temperature is equal to

$$Tres = \frac{1}{0.04 \cdot 2^N \cdot \frac{R_{SENSOR,TNOM}}{R_C} \cdot TC_{RS}} \tag{6}$$

Assuming:

- An Rc value of 100Ohms- 5 VCS331Z (VISHAY company) resistors in parallel with a TC of 0.05ppm, which in our case can be neglected because it is very small.
- A temperature coefficient of the PT1000 PTC equal to 0.385Ohm/degC
- 14 bits of ADC operation

a temperature resolution of 0.039 deg C is achieved. For lower resolution applications a 10 bit configuration could be used. In this case a 0.63 deg C temperature resolution is achieved.
The maximum and minimum temperature differences that can be achieved with this configuration can be calculated from eq.4 by substituting OC with OCmax=2N. The maximum temperature range is 384 deg C.
The user can place another sensor (other than the PT1000). However, the methodology for selecting the component values, as derived from eq.1-6, remains the same.

16.2 TID Measurements with pSIF

As in the case of temperature measurements, the pSIF device can be used for TID monitoring through a RADFET. The only differences with the temperature measurement mode are that

- Instead of a temperature sensor, a RADFET is connected at the current source output
- The output current value has to be set at the range of 1-5uA. Thus, the value of Rc has to be in the range of 20-100K. Again low temperature coefficient resistors from VISHAY can be used.
- A power supply independent voltage is connected at node CS_V+_R1.

The setup for TID monitoring is shown in Fig. 23. The RADFET that is advised to be used is the 100nm RADFET from NMRC (Ireland). As far as bias connections

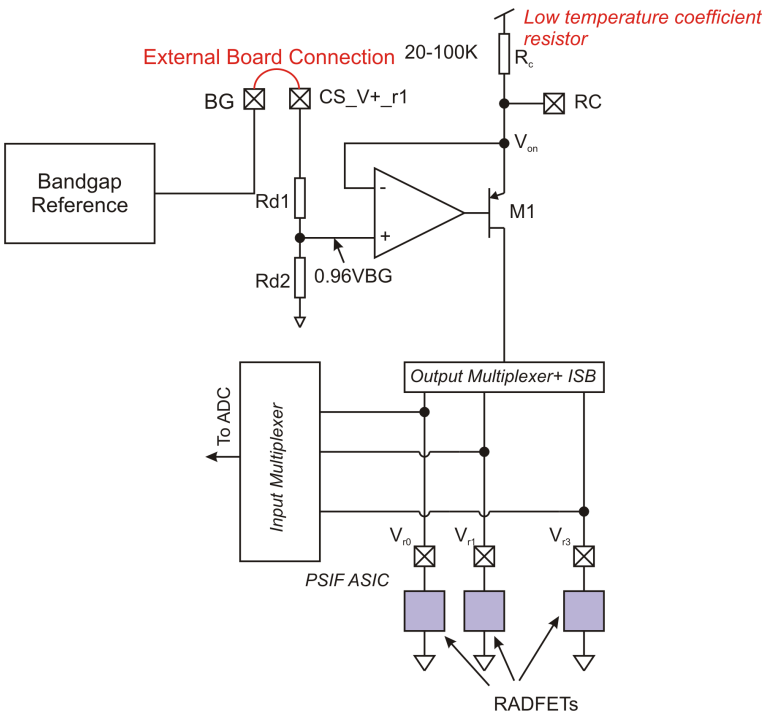

Figure 23: Setup for using the pSIF for TID measurements utilizing the current source and an external low temperature coefficient resistor.

are concerned, the same recommendation as in section 2.3 apply.

16.3 Using pSIF for Single Ended Voltage Measurements

The core element of the pSIF device is its 14bit 1Mrad rad hard ADC. Thus, pSIF can be used for relatively high precision voltage measurements. In this case the entire analog front end can be biased off and the user has direct access to the ADC through the VR nodes as shown in Fig. 24.

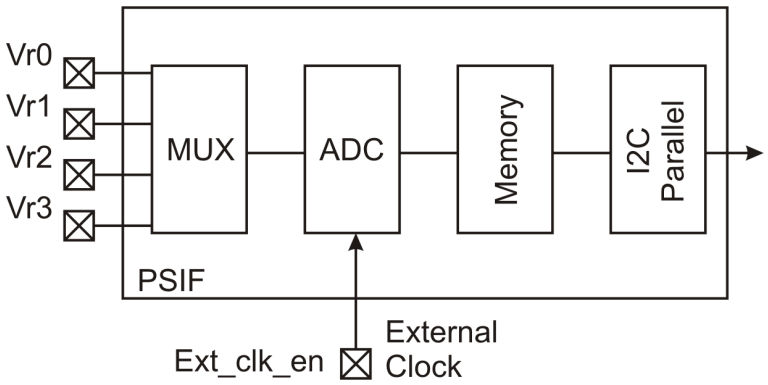

Figure 24: Setup for using the pSIF for performing single ended voltage measurements.

In addition a single ended amplification can be applied to the input. In this case the setup is shown in Fig. 25

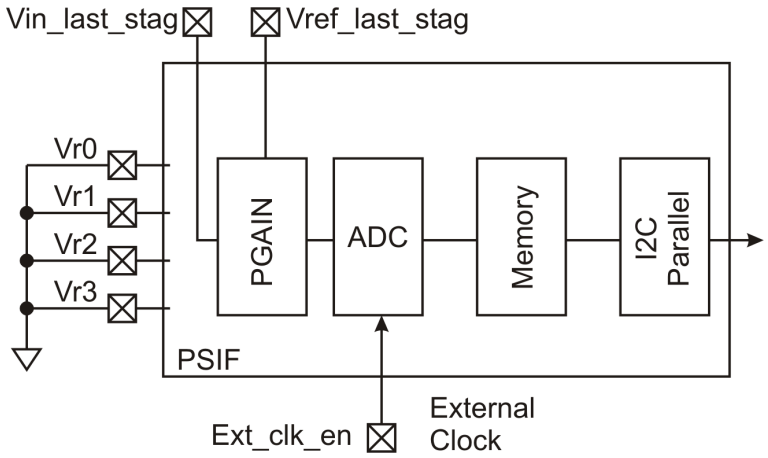

Figure 25: Setup for using the pSIF for performing single ended voltage measurements with amplification.

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